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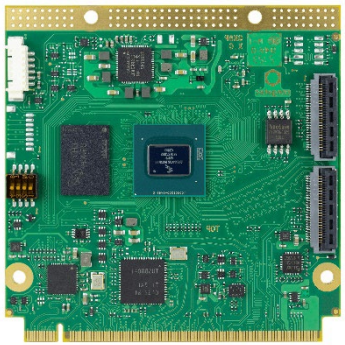
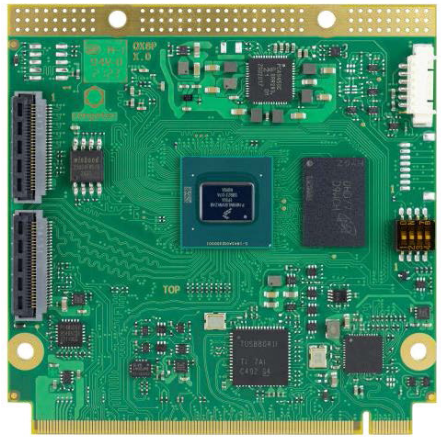
Qseven 2.1 COM, NXP i.MX 8M Plus 14nm processor series with ARM 4-Core Cortex-A53 / M7 + NPU





Qseven® conga-QMX8-Plus

Qseven® 2.1 module based on the NXP® i.MX 8M Plus applications processors

User's Guide

Revision 0.1 (Preliminary)

congatec

Revision History

Revision	Date (yyyy-mm-dd)	Author	Changes
0.1	2022-02-15	BEU	• Preliminary release

Preface

This user's guide provides information about the components, features and connectors available on the conga-QMX8-Plus. It is one of five documents that should be referred to when designing an NXP® i.MX 8M Plus based Qseven® application. The other reference documents that should be used include the following:

conga-QMX8-Plus Pinout (see section 7 "Signal Descriptions and Pinout Tables")
Qseven® Design Guide 2.0 (www.sget.org)
Qseven® Specification 2.1 (www.sget.org)
NXP® i.MX 8M Plus Applications Processor Datasheet for Industrial Products (www.nxp.com)

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Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

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Terminology

Term	Description
°C	Degrees Celsius
µA	Microamp
µs	Microsecond
A	Ampere
AN	Application Note
ARM	Advanced RISC Machine
AVB	Audio Video Bridging
BT	Bluetooth
CAAM	Cryptographic Acceleration and Assurance Module
CMOS	Complementary Metal Oxide Semiconductor
COM	Computer-on-Module
CPU	Central Processing Unit
CSI	Camera Serial Interface
CSP	Cooling Solution Passive
DDR	Double Data Rate
DP	DisplayPort
DP++	DisplayPort Dual-Mode
DRAM	Dynamic Random Access Memory
DSI	Display Serial Interface
D-SUB	D-Subminiature
eMMC	embedded MultiMediaCard
eSPI	enhanced Serial Peripheral Interface
FlexCAN	Flexible Controller Area Network
GB	Gigabyte
GbE	Gigabit Ethernet
GHz	Gigahertz
GND	Ground
GPIO	General-Purpose Input/Output
GPU	Graphics Processing Unit
GTps	Gigatransfers per second
HDMI	High-Definition Multimedia Interface
HW	Hardware
HAB	High Assurance Boot
HSP	Heat Spreader
Hz	Hertz
I/O	Input/Output
I²C (I2C)	Inter-Integrated Circuit
I²S (I2S)	Inter-Integrated Circuit Sound
IEEE	Institute of Electrical and Electronics Engineers
JEIDA	Japan Electronic Industries Development Association
JTAG	Joint Test Action Group
KS	Key State
LPDDR	Low-Power Double Data Rate
LVDS	Low-Voltage Differential Signaling
Mbps	Megabits per second
MBps	Megabytes per second
MHz	Megahertz
mm	Millimeter
MMU	Memory Management Unit
mVpp	Millivolts Peak to Peak
MXM	Mobile PCI Express Module
NC	Not Connected
Nm	Newton metre
NXP	NeXt exPerience
OS	Operating System
OTG	On-The-Go
PCB	Printed Circuit Board
PCI Express	Peripheral Component Interconnect Express
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PN	Part Number
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit-Media Independent Interface
RS-232	Recommended Standard 232
RTC	Real-Time Clock
SAI	Synchronous Audio Interface
SD	Secure Digital
SDIO	Secure Digital Input Output
SDR	Single Data Rate
SDRAM	Synchronous Dynamic Random Access Memory
SDXC	Secure Digital eXtended Capacity
SGET	Standardization Group for Embedded Technologies e.V
SMARC	Smart Mobility ARChitecture
SoC	System on Chip
SNVS	Secure Non-Volatile Storage
SPI	Serial Peripheral Interface
TBD	To Be Defined
TMU	Thermal Management Unit
UART	Universal Asynchronous Receiver-Transmitter
U-Boot	Universal Boot Loader
UHS	Ultra High Speed
USB	Universal Serial Bus
uSDHC	Ultra Secure Digital Host Controller
V	Volt
Vdc	Volts direct current
VESA	Video Electronics Standards Association
W	Watt
Wi-Fi	Wireless Fidelity

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List of Tables

1 Introduction

1.1 Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Computer-On-Module that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and a specified pinout based on the high speed MXM system connector. The pinout remains the same regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network interface and multiple USB ports.

A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express® graphics cards in notebooks.

Carrier board designers can use as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration.

The conga-QEVAL/Qseven® 2.0 evaluation carrier board provides carrier board designers with a reference design platform and the opportunity to test all the Qseven® I/O interfaces available and then choose what are suitable for their application. Qseven® applications are scalable, which means once a carrier board has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no need to redesign the carrier board.

1.2 conga-QMX8-Plus

The conga-QMX8-Plus is a Computer On Module (COM) based on the Qseven® Hardware Specification 2.1. The conga-QMX8-Plus features an NXP® i.MX 8M Plus applications processor with four Arm® Cortex®-A53 processor cores, one Arm® Cortex®-M7 processor and an integrated 2.3 TOPS Neural Processing Unit (NPU) for machine learning applications. The System on Chip (SoC) is manufactured using the 14nm LPC FinFET technology for high computing performance at low power. The conga-QMX8-Plus only requires 2 - 5 W @ 5V for typical applications.

By offering most of the functional requirement for any Qseven® application, the conga-QMX8-Plus provides manufacturers and developers with a platform to jump-start the development of systems and applications based on Qseven® Hardware Specification. Its features and capabilities make it an ideal platform for designing compact, energy-efficient, performance-oriented embedded systems.

1.3 Options Information

The conga-QMX8-Plus is currently available in two commercial and two industrial variants. The two tables below show the base configuration modules that are currently offered by congatec GmbH.

Table 1 Commercial Variants

PN	016600	016601
NXP® Processor	i.MX 8M Plus Quad	i.MX 8M Plus Quad
Cortex®-A53	4x 1.8 GHz	4x 1.8 GHz
DRAM	4 GB LPDDR4 @ 2000 MHz (32 bit) with In-line ECC	2 GB LPDDR4 @ 2000 MHz (32 bit) with In-line ECC
eMMC	16 GB	16 GB

Table 2 Industrial Variants

PN	016620	016621
NXP® Processor	i.MX 8M Plus Quad	i.MX 8M Plus Quad
Cortex®-A53	4x 1.6 GHz	4x 1.6 GHz
DRAM	4 GB LPDDR4 @ 2000 MHz (32 bit) with In-line ECC	2 GB LPDDR4 @ 2000 MHz (32 bit) with In-line ECC
eMMC	16 GB	16 GB

1.4 Accessories

Table 3 Accesories

PN	Product Name	Description
007005	conga-QEVAL/Qseven 2.0 ARM	Evaluation carrier board for Qseven® ARM modules.
500025	conga-HDMI add-on card	conga-HDMI add on card is used for evaluation of the HDMI® graphics interface of Qseven® modules in combination with the congatec evaluation carrier board conga-QEVAL.
48000023	RS232 adapter cable for conga-ARM modules	RS232 adapter cable for congatec ARM modules console debug application
44500041	Basler dart camera daA3840-30mc	Basler dart BCON for MIPI camera module daA3840-30mc, 8Mpx, 30fps, 4 CSI2-Lanes, S-Mount
10000399	FFC Basler dart BCON for MIPI, 200mm	FFC 28 pin cable for Basler BCON dart cameras, 0,5mm pitch. compatible with 28 pin Hirose ZIF connector (PN: FH41-28S-0.5SH(05))
10000429	Evetar Lens M118B0418IR F1.8 f4mm 1/1.8" - Lens	Evetar Lens M118B0418IR F1.8 f4mm 1/1.8" - Lens for Basler dart camera module daA3840-30mc

2 Specifications

2.1 Feature List

Table 4 Feature Summary

Form Factor	Qseven® Specification 2.1
SoC	NXP® i.MX 8M Plus Quad: 4x Arm® Cortex®-A53 cores @ 1.8 GHz (commercial) or 1.6 GHz (industrial) | 1x Arm® Cortex®-M7 @ 800MHz | NPU 2.3 TOPS | GPU GC7000UL
DRAM	Up to 6 GByte onboard LPDDR4 memory | 4000 MT/s | In-line ECC
AI & Machine Learning	Neural Processing Unit (NPU) with up to 2.3 TOPS | NXP® eIQ Machine Learning SW tools and libraries
Ethernet	1x Gbit Ethernet with IEEE 1588 and TSN Support
I/O Interfaces	1x dual-role USB 3.0 3x USB 2.0 1x USB 3.0 1x SDIO 3.0 1x onboard µSD card socket 1x PCIe® 3.0 2x I²C 1x SPI 1x UART with Handshake 1x CAN FD 12x GPIOs
Mass Storage	eMMC 5.1 up to 128 GByte | SPI NOR Flash up to 32 MByte
Sound	1x I²S | HiFi 4 DSP
Graphics	Integrated in SoC | GC7000UL 3D graphics with 2 high performance vec4 shaders | GC520L 2D graphics VPU up to 1080p60 H.265/H.264 decoding and encoding | OpenGL ES 3.1 | Vulcan | OpenCL 1.2 FP | OpenVG 1.1 | 2 independent displays
Video Interfaces	1x dual channel 24-bit LVDS 1x MIPI-DSI 4-lane shared with second LVDS channel (optional) 1x HDMI 2.0a Up to 2x MIPI-CSI 4-lane onboard connectors 2x integrated Image Signal Processor (ISP) for cameras with up to 12 MP
Features	Watchdog Timer | Cortex®-A53 Console | optional JTAG debug interface | High Precision Real Time Clock
Security	Cryptographic Acceleration and Assurance Module (CAAM) | Resource Domain Controller | ARM® TrustZone® High Assurance Boot support | Encryption Engine AES-128/192/256, DES/3DES, RC4, RSA4096, TRNG SHA-1/244/256, MD-5 | RSA-1024, 2048, 3072, 4096 and secure key storage | side channel attack resistance
Boot Loader	U-Boot boot loader
Operating Systems	Linux® (Yocto Project®) | Android™
Power Consumption	Typical application 2-5W @ 5V
Temperature Range	Operating Temperature Range: 0 to +60°C commercial grade | -40 to +85°C industrial grade Storage Temperature Range: -40 to +85°C
Humidity	Operating: 10 to 90% r. H. non cond. | Storage: 5 to 95% r. H. non cond.
Size	70 mm x 70 mm

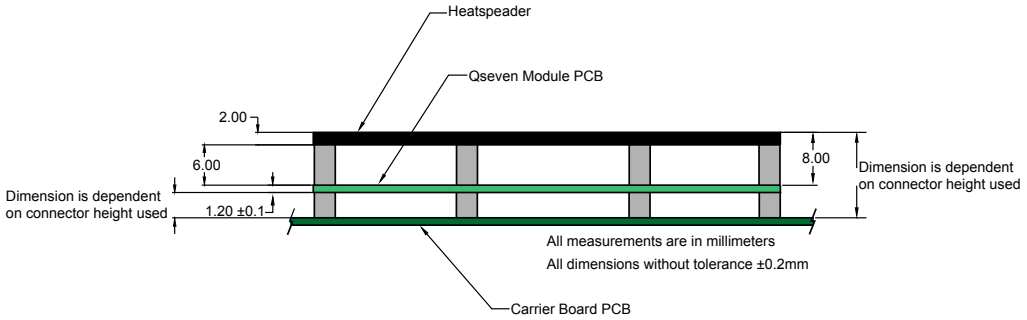
2.2 Supported Operating Systems

The conga-QMX8-Plus supports the following operating systems:

- Linux® (Yocto Project®)
- Android™

2.3 Mechanical Dimensions

- 70.0 mm x 70.0 mm
- The Qseven® module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12 mm thick.

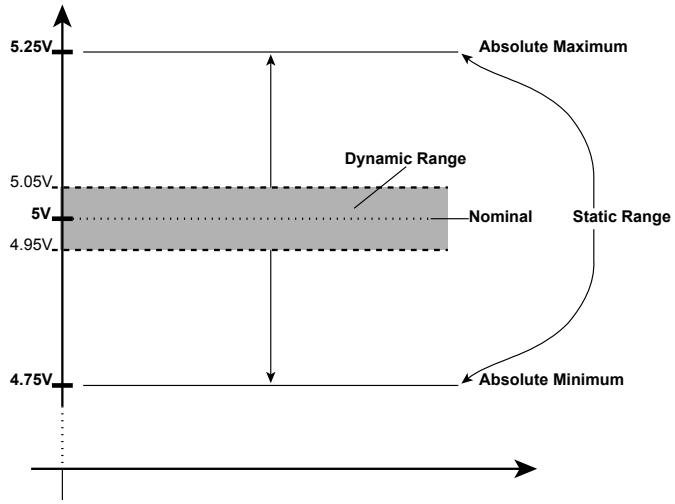


Rear View of Qseven Module

2.4 Supply Voltage Standard Power

- 5V DC ± 5%

The dynamic range shall not exceed the static range.



2.4.1 Electrical Characteristics

Characteristics			Min.	Typ.	Max.	Units	Comment
5V	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple		-	-	± 50	mV_{PP}	0-20MHz
	Current						
5V_SB	Voltage	± 5%	4.75	5.00	5.25	Vdc	
	Ripple				± 50	mV_{PP}	

2.4.2 Rise Time

The input voltages shall rise from 10 percent of nominal to 90 percent of nominal at a minimum slope of 250 V/s. The smooth turn-on requires that, during the 10 percent to 90 percent portion of the rise time, the slope of the turn-on waveform must be positive.

Note

For information about the input power sequencing of the Qseven® module, refer to the Qseven® specification.

2.5 Power Consumption

The power consumption values were measured with the following setup:

- Input voltage +5 V
- conga-QMX8-Plus
- conga-QEVAL carrier board
- conga-QMX8-Plus cooling solution

The power consumption values were recorded during the following operating modes:

Table 5 Measurement Description

System State	Description	Comment
Suspend	Dormant mode / Deep sleep mode	For more information about these states, refer to the Application Note "i.MX 8M Plus Power Consumption Measurement" available at the NXP® website www.nxp.com.
Idle	System idle mode	
100% Workload	100% CPU workload	The CPU was stressed to its maximum frequency.
Peak Power Consumption	100% CPU workload at approximately 100°C peak power consumption	Consider this value when designing the system's power supply to ensure that sufficient power is supplied during worst case scenarios.

Note

The peripherals did not influence the measured values because they were powered externally.

The table below provides the power consumption values of each conga-QMX8-Plus variant during different operating modes:

Table 6 Power Consumption Values

PN	Memory Size	HW Revision	U-Boot	SoC	Current (A) @ 5 V			
					Suspend	Idle	100% Workload	Peak Power Consumption
016600	4 GB	TBD	TBD	i.MX 8M Plus Quad (1.8 GHz)	TBD	TBD	TBD	TBD
016601	2 GB	TBD	TBD	i.MX 8M Plus Quad (1.8 GHz)	TBD	TBD	TBD	TBD
016620	4 GB	TBD	TBD	i.MX 8M Plus Quad (1.6 GHz)	TBD	TBD	TBD	TBD
016621	2 GB	TBD	TBD	i.MX 8M Plus Quad (1.6 GHz)	TBD	TBD	TBD	TBD

2.6 Supply Voltage Battery Power

- 2.0V-3.6V DC
- Typical 3V DC

2.6.1 CMOS Battery Power Consumption

Table 7 CMOS Battery Power Consumption

RTC @	Voltage	Current
-10°C	3V DC	TBD µA
20°C	3V DC	TBD µA
70°C	3V DC	TBD µA

Note

1. *Do not use the CMOS battery power consumption values listed above to calculate CMOS battery lifetime.*
2. *Measure the CMOS battery power consumption in your customer specific application in worst case conditions (for example, during high temperature and high battery voltage).*
3. *Consider the self-discharge of the battery when calculating the lifetime of the CMOS battery. For more information, refer to application note AN9_RTC_Battery_Lifetime.pdf at www.congatec.com/support/application-notes*

Note

To improve the lifetime of the CMOS battery, congatec implemented an external real-time clock onboard the conga-QMX8-Plus module.

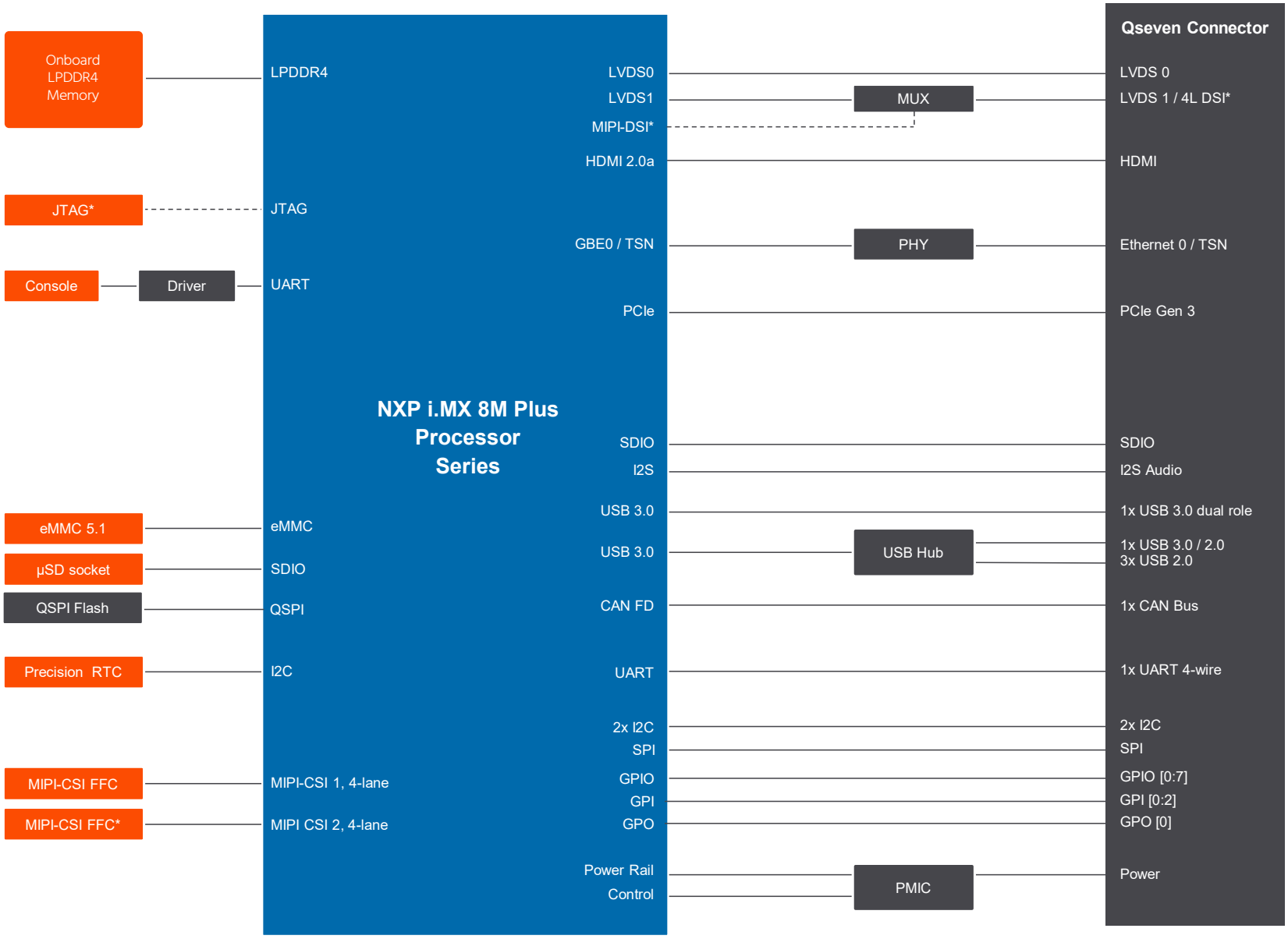
2.7 Environmental Specifications

Temperature (commercial variants)	Operation:	0° to 60°C	Storage: -40° to +85°C
Temperature (industrial variants)	Operation:	-40° to 85°C	Storage: -40° to +85°C
Humidity	Operation:	10% to 90%	Storage: 5% to 95%

Caution

1. *The above operating temperatures must be strictly adhered to at all times. When using a congatec heatspreader, the maximum operating temperature refers to any measurable spot on the heatspreader's surface.*
2. *Humidity specifications are for non-condensing conditions.*

3 Block Diagram



* Assembly Option

4 Heatspreader

congatec GmbH offers the following heatspreader variants for the conga-QMX8-Plus. Each heatspreader variant is intended for specific module variants as shown in the table below. The dimensions of the heatspreader are shown in the sub-sections. All measurements are in millimeters.

Table 8 Heatspreader Variants

Heatspreader Variant	Heatspreader Part No. (PN)	Compatible conga-QMX8-Plus Variants (PN)	Description
conga-QMX8-Plus/HSP-T	016650	016620, 016621	Standard heatspreader for Qseven module conga-QMX8-Plus with NXP i.MX 8M Plus ARM processor. All standoffs are M2.5 thread.
conga-QMX8-Plus/HSP-B	016651	016620, 016621	Standard heatspreader for Qseven module conga-QMX8-Plus with NXP i.MX 8M Plus ARM processor. All standoffs are with 2.7mm bore hole.

Note

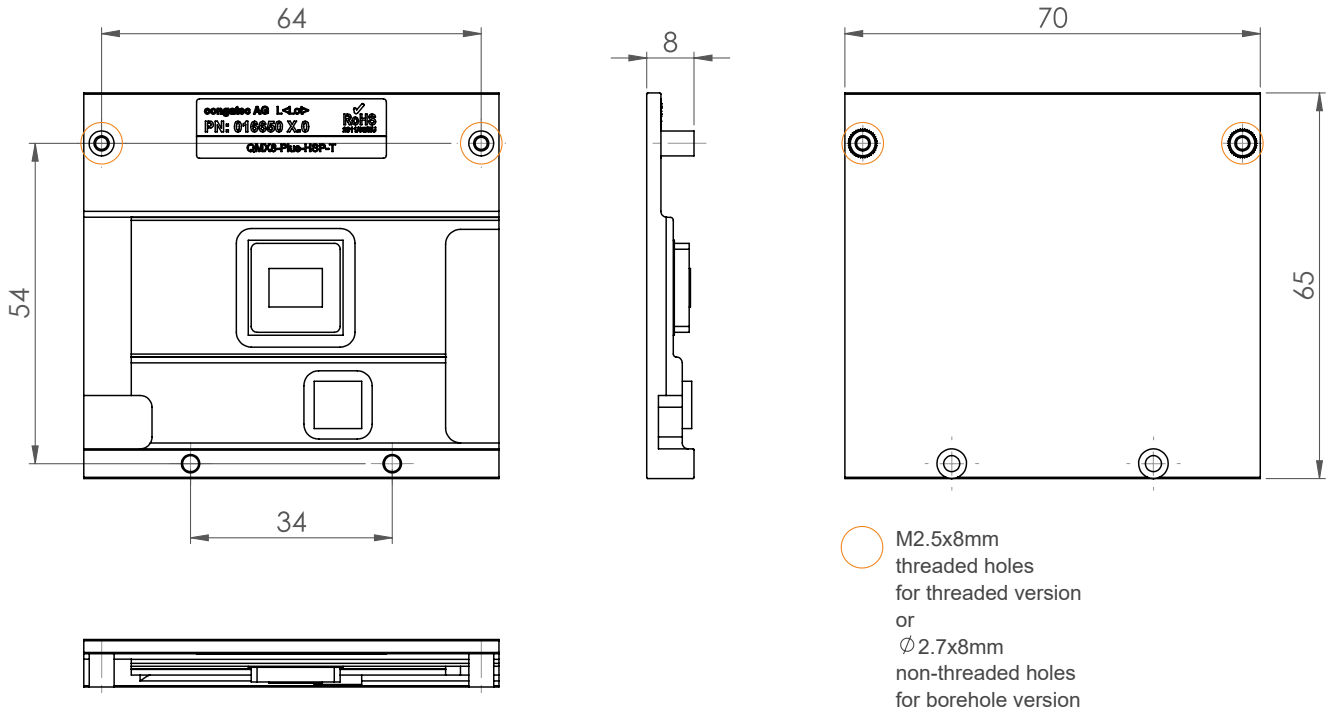
1. *We recommend a maximum torque of 0.4 Nm for carrier board and module mounting screws.*
2. *The gap pad material used on congatec heatspreaders may contain silicon oil that can seep out over time depending on the environmental conditions it is subjected to. For more information about this subject, contact your local congatec sales representative and request the gap pad material manufacturer's specification.*
3. *Only a few NXP® i.MX 8M Plus on-chip devices are enabled by default in the bootloader. With this default configuration, the power consumption is low. However, power consumption may increase significantly depending on your application and the workload.*

Caution

1. *The congatec heatspreaders/cooling solutions are tested only within the commercial temperature range of 0° to 60°C. Therefore, if your application that features a congatec heatspreader/cooling solution operates outside this temperature range, ensure the correct operating temperature of the module is maintained at all times. This may require additional cooling components for your final application's thermal solution.*
2. *For adequate heat dissipation, use the mounting holes on the cooling solution to attach it to the module. Apply thread-locking fluid on the screws if the cooling solution is used in a high shock and/or vibration environment. To prevent the standoff from stripping or cross-threading, use non-threaded carrier board standoffs to mount threaded cooling solutions.*
3. *For applications that require vertically-mounted cooling solution, use only coolers that secure the thermal stacks with fixing post. Without the fixing post feature, the thermal stacks may move.*
4. *Do not exceed the recommended maximum torque. Doing so may damage the module or the carrier board, or both.*

4.1 Heatspreader Dimensions

PN: 016650, 016651



5 Connector Subsystems

The conga-QMX8-Plus is based on the Qseven® standard and therefore has 115 edge fingers on the top and bottom side of the module that mate with the 230-pin card-edge MXM connector located on the carrier board. This connector provides the ability to interface the available signals of the conga-QMX8-Plus with the carrier board peripherals.

5.1 PCI Express®

The conga-QMX8-Plus offers one PCI Express® (PCIe®) lane. The PCIe® signals are routed from the NXP® i.MX 8M Plus processor to the PCIe® port 0 of the conga-QMX8-Plus edge finger. These signals support PCI Express Gen 3 interfaces at 8 Gb/s and are backward compatible to Gen 2 interfaces at 5 Gb/s and Gen 1.1 interfaces at 2.5 Gb/s. The PCIe® reference clock is generated by an onboard precision oscillator (Microchip DSC557-03). Only x1 PCIe® link configuration is possible.

5.2 UART/RS-232

The conga-QMX8-Plus offers one UART interface on the MXM connector and two RS-232 interface onboard by default. The UART offered on the MXM connector is fully featured with control signals (4 pin UART) and is connected directly to UART1 port of the NXP® i.MX 8M Plus Cortex®-A53 processor.

The onboard RS-232 interfaces are offered via a 6-pin Molex connector. The signals are provided by routing the UART2 and UART4 pins of the NXP® i.MX 8M Plus processor to a MA3232 transceiver. The transceiver converts the UART CMOS level (3.3V) to RS-232 voltage levels and is guaranteed to run at data rates of 250 kbps in the normal operating mode, while maintaining RS-232 output levels. With the Molex connector, you can output data to the console by using the appropriate RS-232 adapter cable. For more information, refer to section 6.1 "UART/RS-232 Debug Port".

The UART interfaces support 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none), programmable baud rates up to 4 Mbps, 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.

Table 9 Overview of UART/RS-232 Ports

SoC	Qseven® Pins	Onboard Connector (X4)
UART1	UART0	
UART2	MFG (Optional) / RSVD Pins 54 and 55 (Assembly Option)	Cortex®-A53 Console (Default)
UART3	GPIO (Optional)	
UART4	RSVD Pins 52 and 53 (Assembly Option)	Cortex®-M7 Debug (Default)

Note

1. *The UART interface on the MFG pins can be realized as described in the Qseven® Specification.*
2. *The MFG_NC4 pin is high active and has an internal pull down resistor on the conga-QMX8-Plus module. This means that the MFG pins on the edge connector functions as UART interface by default.*
3. *The UART interface on the GPIO pins is described in section 5.9 "LPC/GPIO".*
4. *The UART interfaces on the onboard connector X4 are described in section 6.1 "UART/RS-232 Debug Port".*

5.3 Gigabit Ethernet

The conga-QMX8-Plus offers Gigabit Ethernet via an onboard TI DP83867IS Physical Layer (PHY). This PHY is implemented via the RGMII interface of the NXP® i.MX 8M Plus processor. The Ethernet interface consists of 4 pairs of low voltage differential pair signals designated from GBE0_MDI0± to GBE0_MDI3± plus control signals for link activity indicators. These signals can be used to connect to a 10/100/1000 BaseT RJ45 connector with integrated or external isolation magnetics on the carrier board.

The Gigabit Ethernet interface supports:

- 10/100/1000 Mbps
- Energy Efficient Ethernet (EEE)
- Ethernet AVB
- IEEE 1588v2 Precision Timing Protocol (PTP)
- Time Sensitive Networking (TSN)

Note

The 1588 event or triger signal is routed to Qseven® pin 124 "GP_1-Wire_Bus / HDMI_CEC".

5.4 SATA

The NXP® i.MX 8M Plus Cortex®-A53 processor does not support SATA. Therefore, the conga-QMX8-Plus does not support SATA.

5.5 USB

The conga-QMX8-Plus offers five USB ports via two USB 3.0 controllers with integrated PHY controllers provided by the NXP® i.MX 8M Plus Cortex®-A53 processor. These controllers provide USB functionality that comply with the USB 3.0 and USB 2.0 specification. OTG is not supported.

The offered ports comprise of two USB 3.0 (5 Gbps) ports, one of which is Dual-Role capable, and three USB 2.0 ports. One USB 3.0 ports and the three USB 2.0 ports are derived through the integration of a TI TUSB8041 USB hub, and are implemented by routing the USB2 port of the processor to the TI hub. The Dual-Role capable USB 3.0 port is connected directly to the USB1 port of the NXP® i.MX 8M Cortex®-A53 processor.

Table 10 Overview of USB Ports

Qseven	Default	Assembly Option (Without USB Hub)
USB_P0	USB 3.0 (5 Gbps)	USB 3.0 (5 Gbps)
USB_P1	USB 3.0 Dual-Role	USB 3.0 Dual-Role
USB_P2	USB 2.0	N/A
USB_P3	USB 2.0	N/A
USB_P4	USB 2.0	N/A

Note

USB_P1 can be used for the Serial Downloader mode. Fore more information, see section 5.18.1 "Serial Downloader Mode".

5.6 SD/SDIO/MMC

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card or MMC-Card flash memories. The SD/SDIO/MMC cards communicate with the host system via the Ultra Secured Digital Host Controller (uSDHC). This controller acts as a bridge by sending commands and accessing data to and from the cards. The NXP® i.MX 8M Plus processor on the conga-QMX8-Plus provides three SD/SDIO/MMC controllers for communicating with different SD, SDIO and MMC devices.

The conga-QMX8-Plus offers one SDIO interface on the MXM connector via the NXP® i.MX 8M SDHC1 port. Two other SDIO ports provided by the NXP® i.MX 8M Plus processor are supported onboard the conga-QMX8-Plus. These ports (SD2 and SD3) connect the onboard 4 bit micro SD card socket and the onboard 8 bit eMMC respectively.

The SD/SDIO interface on the MXM connector supports:

- OS boot (U-Boot not supported)
- SD/SDIO specification 3.0
- 200 MHz 1.8V signaling for up to 100 MBps
- Secure Digital eXtended Capacity (SDXC™) cards
- UHS-I (SDR104/50 and DDR50)
- Default Mode and High Speed Mode

5.7 HDA/I2S/AC'97

The conga-QMX8-Plus uses the Inter-IC Sound (I²S) format for audio signals. These signals are derived from the Synchronous Audio Interface module 5 (SAI5) of the NXP® i.MX 8M Plus processor. This module provides a full duplex serial port that allows communication with external devices using a variety of serial protocols. The I²S protocol is part of the protocols supported by the NXP® i.MX 8M Plus Cortex®-A53 processor.

Note

The conga-QMX8-Plus supports only I2S format.

5.8 Display Interfaces

The conga-QMX8-Plus supports up to two independent displays as listed in the table below:

Table 11 Overview of Display Interfaces

	Display 1		Display 2		Display 3	
	Interface	Max. Resolution	Interface	Max. Resolution	Interface	Max. Resolution
Default	Dual channel LVDS	1920x1080p60	-	-	HDMI®	3840x2160p30
Assembly Option			MIPI DSI®	2560x1080p60	HDMI®	3840x2160p30

Note

The MIPI® DSI interface only supports max. resolution 2560x1080p60 if it is the only display interface in use. Otherwise, the MIPI® DSI interface supports max. resolution 1920x1200p60.

5.8.1 LVDS and optional MIPI DSI®

The conga-QMX8-Plus offers LVDS_[A:B] pins for one 18 / 24 bit dual channel LVDS interface by default.

Optionally, the LVDS_B pins can be used for a one 4-lane MIPI DSI® interface instead (assembly option).

Note

The conga-QMX8-Plus does not support eDP™.

5.8.2 HDMI®

The conga-QMX8-Plus offers pins for one High-Definition Multimedia Interface (HDMI®) 2.0a display interface with support for multi-channel audio output. The supported resolutions are 720x480p60, 1280x720p60, 1920x1080p60, 1920x1080p120, and 3840x2160p30.

HDMI® is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI® encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video.

The conga-QMX8-Plus provides HDMI® connection directly from the NXP® i.MX 8M Plus processor. Video data is provided through three differential TMDS data pairs (TMDS_LANE0± to TMDS_LANE2±) and one differential clock pair (TMDS_CLK±). In addition, HDMI® includes a DDC (Digital Display Channel) interface for the configuration exchange and Hot plug detection signal.

5.9 LPC/GPIO

The conga-QMX8-Plus does not support the Low Pin Count (LPC) signals, instead eight General-Purpose Input/Output (GPIO) pins shared with the LPC pins according to Qseven® Specification 2.1 are supported.

The General Purpose Input/Output pins can be configured as inputs or outputs. When configured as output, it is possible to write to an internal register to control the state driven on the output pin. When configured as input, the input state can be detected by reading the status of an internal register. To select the GPIO mode, configure the IOMUX.

The conga-QMX8-Plus offers GPIO[0:7] pins for GPIO use with support for alternate functions as listed in the table below:

Table 12 Overview of GPIO[0:7] Pins

Signal Name	Pin	Primary Function	PU / PD	Alternative Use 1	Alternative Use 2
GPIO0	185	GPIO Pin 0	socPD-22k	SPI1_MOSI	
GPIO1	186	GPIO Pin 1	socPU-22k	SPI1_CS0#	
GPIO2	187	GPIO Pin 2	socPD-22k	SPI1_MISO	
GPIO3	188	GPIO Pin 3	socPD-22k	SPI1_SCLK	
GPIO4	189	GPIO Pin 4	socPD-22k	I2S0_MCLK	
GPIO5	190	GPIO Pin 5	socPU-22k	CAN1_RX	UART3_RX
GPIO6	191	GPIO Pin 6	socPD-22k	ENET_1588_IN	
GPIO7	192	GPIO Pin 7	socPU-22k	CAN_TX	UART3_TX

5.10 SPI

The NXP® i.MX 8M Plus processor provides Enhanced Configurable Serial Peripheral Interfaces (ECSPIs). The ECSPI interfaces offer full-duplex, synchronous serial interface with maximum operation frequency for read operations of up to 25 MHz and up to 50 MHz for write operations. It can be configured to support Master/Slave modes and support multiple peripherals via chip selects.

The conga-QMX8-Plus offers SPI pins for one Serial Peripheral Interface (SPI) with two device chip selects via the SPI_CS[0:1]# pins on the edge finger connector. This SPI is connected to ECSPI2 of the NXP® i.MX 8M Plus processor. The FlexSPI interface from the NXP® i.MX 8M Plus processor is connected to the 64 Mbit SPI Flash memory onboard the conga-QMX8-Plus. The NXP® i.MX 8M Plus processor is programmed to boot from the bootloader contained in the SPI flash memory.

Optionally, the conga-QMX8-Plus can offer an additional SPI via GPIO pins on the edge finger connector. This SPI is connected to ECSPI1 of the NXP® i.MX 8M Plus processor. For more information, see section 5.9 "LPC/GPIO".

5.11 CAN Bus

The conga-QMX8-Plus offers CAN0 pins for one Controller Area Network (CAN) buses via the FlexCAN1 controller integrated in the NXP® i.MX 8M Plus processor. The bus supports the CAN FD and CAN 2.0 B protocols. To connect the CAN controller module to the CAN bus, it is necessary to add transceiver hardware. A complete description of the CAN controller registers and functionality is beyond the scope of this user's guide. Consult NXP's i.MX 8M Plus processor reference manual for additional information about this interface.

Optionally, the conga-QMX8-Plus can offer an additional CAN bus via GPIO pins on the edge finger connector. The additional CAN bus is provided via the FlexCAN2 controller integrated in the NXP® i.MX 8M Plus processor. For more information, see section 5.9 "LPC/GPIO".

5.12 Manufacturing/JTAG Interface

The manufacturing signals defined in Qseven® Specification 2.1 are reserved for either manufacturing or debugging purposes. Optionally, the conga-QMX8-Plus offers this interface as a 10-pin JTAG interface for debugging purposes (assembly option). This interface is connected to the JTAG controller of the NXP® i.MX 8M Plus processor. The JTAG control fuses are used to allow or disallow JTAG access to secured resources. For more information, refer to section 6.3 "JTAG Interface".

5.13 Power Control

PWRBTN#

Active low input signal with 22k pull up resistor on the module, usually used to connect a push-button. A short power button event initiates the transition between SNVS and RUNTIME power states (controlled by operating system). A long power button event initiates the transtition from RUNTIME to SNVS power state (controlled by hardware).

SUS_S5# (PWR_ON_REQ)

Output signal used to control (1=enable/0=disable) VCC power rail for the module and also rest power rails on carrier board. When this signal is low, input signals to the module should **NOT** be driven high—with the exception of PWRBTN# and others Qseven® suspend signals. SUS_S5# (PWR_ON_REQ) is low in the OFF and SNVS power states and high in the RUNTIME and SUSPEND power states.

SUS_S3# (PWR_STBY_REQ#)

Output signal used to control (1=enable/0=disable) power rails on the carrier board that supply runtime power to interfaces and devices. SUS_S3# (PWR_STBY_REQ#) is low in the OFF, SNVS, and SUSPEND power states and high in the RUNTIME power state.

Note

Optionally, the module can keep SUS_S3# (PWR_STBY_REQ#) high during the SUSPEND power state (software option). This option is intended for cases where VCC for the module is controlled by SUS_S3# on the carrier board.

PWGIN

Power good input signal with pull up resistors on the module, used to indicate that VCC is stable and the module can start to boot. PWGIN should be driven by an open-drain output on the carrier board. A push-pull is also accetable. If it is not required to delay the start of the boot process, this signal can be floating. A voltage monitor for the VCC power rail is implemented on the module. The PWGIN signal must **NOT** be driven to low in the SUSPEND power state. Optionally, this signal can be disconnected on the module (assembly option).

Note

The RSTBTN# input signal can also be used to delay the start of the boot process.

Note

The conga-QMX8-Plus boots up immediately power is applied to the module's +5V input rail and PWGIN is active (if used). To shutdown the system, use the the linux command "poweroff". Depending on the operating system, the shutdown can also be performed by pressing the power button. If the system is in shutdown or standby state, pressing the power button restores the system back to full-on state. When the chip main power supply is Off, a button press asserts an output signal to request turn on the runtime power rails.

If it is desired to keep the system switched off even when the +5V input power rail is initially powered on (ATX-style), an external logic has to be used that prevents the system from booting by means of the power good signal (PWGIN). It is the responsibility of the external logic to release the PWGIN signal, when the desired event (e.g. pressing the power button) occurs.

Power Supply Implementation Guidelines

5V input power is the sole operational power source for the conga-QMX8-Plus. The remaining necessary voltages are internally generated on the module using onboard voltage regulators.

Note

The input power supply must have a monolithic ramp.

Inrush and Maximum Current Peaks on VCC_5V_SB and VCC

The inrush-current on the conga-QMX8-Plus VCC_5V_SB power rail can go up as high as TBD A for a maximum of 100µS. Sufficient decoupling capacitance must be implemented to ensure proper power-up sequencing.

The maximum peak-current on the conga-QMX8-Plus VCC (5V) power rail can be as high as TBD A. This requires that the power supply be properly dimensioned.

Note

For more information about power control signals refer to the Qseven® Specification.

5.14 Power Management

The NXP® i.MX 8M Plus SoC has an integrated Power Management Unit (PMU) that is used to control power to various SoC/module domains. The table below describes the power states suppoted by the conga-QMX8-Plus:

Table 13 Power States

Power State	Description
OFF	Qseven® power rails VCC_5V_SB and VCC are off. Optionally, the micropower RTC chip is powered by VCC_RTC (if it is supplied).
SNVS	Qseven® power rail VCC_5V_SB is on and VCC is off. All circuits are turned off except the power button event detection and SoC SNVS/RTC logic.
RUNTIME	Qseven® power rails VCC_5V_SB and VCC are on. SoC and module are fully running.
SUSPEND (Deep Sleep)	Qseven® power rails VCC_5V_SB and VCC are on. Cortex®-A53 power is turned off and runtime interfaces/devices on carrier can also be powered off.

5.15 Thermal Management

The NXP® i.MX 8M Plus SoC has two integrated temperature sensors. Both sensors are monitored by the Thermal Management Unit (TMU) which is also integrated in the NXP® i.MX 8M Plus SoC. The TMU offers configurable temperature thresholds for each sensor:

- Exceeding the normal temperature threshold triggers SoC frequency reduction (Default: 95°C)
- Exceeding the critical temperature threshold triggers power off (Default: 105°C)

The main sensor is located inside of the ANAMIX. The second sensor is located near the ARM core.

5.16 Watchdog

The watchdog timer (WDOG) protects against system failures by providing a method of escaping from unexpected events or programming errors. The software must periodically service the watchdog timer once the WDOG is activated. Without the servicing, the timer times out.

5.17 I2C Bus

The Inter-Integrated Circuit (I2C) bus is suitable for applications requiring occasional communications over a short distance between many devices. The I2C interfaces offered by the NXP® i.MX 8M Plus processor support up to 320 kbps, depending on pin loading and timing characteristics

The conga-QMX8-Plus offers two I2C interfaces (I2C2 and I2C3) on the Qseven® edge connector. The I2C2 is connected to the SMBus pins. The I2C3 is conneted to the dedicated Qseven® I2C pins. For more information, refer to the pinout in section 7 "Signal Descriptions and Pinout Tables".

5.18 Boot Select

The onboard SPI flash device is configured as the default boot device via SoC eFuses on conga-QMX8-Plus revisions A.0 and later.

Note

Earlier revisions offer a DIP switch (SW1) onboard the module to select the boot device:

Table 14 Boot Select (Prototype Revisions)

SW1				Selected Boot Source
#4	#3	#2	#1	
OFF	OFF	OFF	OFF	Boot from fuse
OFF	OFF	OFF	ON	Serial download
OFF	OFF	ON	OFF	SDHC3 (eMMC)
OFF	OFF	ON	ON	SDHC2 (uSD onmodule)
OFF	ON	ON	OFF	QSPI (onmodule)

The OS boot device is defined via the U-Boot environment variables. For more information, refer to the conga-QMX8-Plus software documentation linked to in section 8 "Software Documentation".

Optionally, the SoC eFuses can be configured to use a different boot device. The options are onboard eMMC or onboard microSD card socket.

5.18.1 Serial Downloader Mode

Low on the BIOS_DISABLE# / BOOT_ALT# pin enables the Serial Downloader mode. The program image can be downloaded over the USB_P1 port (see section 5.5 "USB"). The conga-QMX8-Plus prototype revisions offer a DIP switch to select the Serial Downloader mode (see section 5.18 "Boot Select").

6 Onboard Interfaces and Devices

6.1 UART/RS-232 Debug Port

The conga-QMX8-Plus is equipped with a six-pin RS-232 connector onboard the conga-QMX8-Plus. It is connected to the NXP® i.MX 8M Plus UART2 and UART4 pins via a MAX3232 transceiver by default. The transceiver is guaranteed to run at data rates of 250kbps in normal operating mode, while maintaining RS-232 output levels. Refer to section 5.2 "UART/RS-232" for more information about the UART interface.

Table 15 UART Signal Descriptions

Pin	SoC Ball	Description
1	UART4_TXD	Cotex®-M7 Debug: Transmit signal via MAX3232 RS-232 Transmitter/Receiver connected to UART4_TXD of the SoC
2	+VIN	Qseven VCC (+5 V)
3	GND	Ground
4	UART2_TXD	Cotex®-A53 Console: Transmit signal via MAX3232 RS-232 Transmitter/Receiver connected to UART2_TXD of the SoC
5	UART2_RXD	Cotex®-A53 Console: Receive signal via MAX3232 RS-232 Transmitter/Receiver connected to UART2_RXD of the SoC
6	UART4_RXD	Cotex®-M7 Debug: Receive signal via MAX3232 RS-232 Transmitter/Receiver connected to UART4_RXD of the SoC

Connector Type

X4: Molex PicoBlade 0532610671 (6 Circuits, 1.25mm Pitch, Right-Angle, Friction Lock)
Mates with Molex PicoBlade Cable Assembly Series 15134 with 6 Circuits

Note

The RS-232 adapter cable for this connector can be ordered from congatec (PN: 48000023 in section 1.4 "Accessories").

6.2 MIPI CSI-2® Camera Connectors

The conga-QMX8-Plus offers one onboard flat foil connector (X2) by default for Basler's proprietary BCON for MIPI interface with four lanes each and up to 1.5 Gbps per lane. X2 is connected to the SoC MIPI-CSI1 interface. For matching camera accessories, refer to the table in section 1.4 "Accessories".

Optionally, conga-QMX8-Plus can offer a second onboard flat foil connector (X3) connected to the SoC MIPI-CSI2 interface (assembly option).

Note

The pinout of the connectors (X2, X3) is not compatible with the optional MIPI-CSI2 feature interface described in the Qseven® Specification.

6.3 JTAG Interface

Optionally, the conga-QMX8-Plus can offer an onboard JTAG debug interface (X5) compatible with Nit6X_JTAG adapter Boundary Devices (assembly option).

Table 16 JTAG Interface Signal Descriptions

Pin	SoC Ball	Description
1	JTAG_VREF	+3.3V sourced by Module
2	JTAG_TMS	JTAG mode select
3	GND	Ground
4	JTAG_TCK	JTAG clock
5	GND	Ground
6	JTAG_TDO	JTAG data out
7	JTAG_MOD	Should not be used
8	JTAG_TDI	JTAG data in
9	GND	Ground
10	JTAG_SRST#	System Reset, active low

Connector Type

X5: Molex PicoBlade 0532611071 (10 Circuits, 1.25mm Pitch, Right-Angle)

6.4 SPI Flash

Onboard the conga-QMX8-Plus is a 64 Mbit SPI flash memory by default. Optionally, the conga-QMX8-Plus can be offered with up to 256 Mbit SPI flash memory (assembly option). This flash memory contains the bootloader and is directly connected to the QSPIA interface of the NXP® i.MX 8M Plus processor.

The NXP® i.MX 8M Plus processor is programmed to boot from the SPI flash by default.

6.5 Android Buttons

Optionally, the conga-QMX8-Plus can offer an onboard eight pin connector (X7) for implementing Android buttons (assembly option). The signals are directly connected to the NXP® i.MX 8M Plus processor. The signals can be only be driven by ground or left open.

Table 17 Android Button Signal Descriptions

Signal	Pin #	Description
PWRBTN#	1	Power button signal
KEY_VOL_UP	2	Increases volume
HOME	3	Returns to the main home screen
SEARCH	4	Brings up the search function
BACK	5	Takes you a level back in an app or a page back in a browser
MENU	6	Displays additional options in an application
KEY_VOL_DN	7	Decreases volume
GND	8	Ground

6.6 LPDDR4 Memory

The conga-QMX8-Plus offers up to 6 GB 32 bit LPDDR4 onboard SDRAM @ 2000 MHz with support for In-band ECC. The default memory size of each conga-QMX8-Plus variant is listed in section 1.3 "Options Information".

6.7 eMMC

The conga-QMX8-Plus offers an onboard eMMC 5.1 HS400 storage device with up to 128 GB (16 GB assembled by default). Changes to the onboard eMMC may occur during the lifespan of the module in order to keep up with the rapidly changing eMMC technology. The performance of the newer eMMC may vary depending on the eMMC technology.

Note

For adequate operation of the eMMC, ensure that at least 15 % of the eMMC storage is reserved for vendor-specific functions.

6.8 Micro SD

The conga-QMX8-Plus offers an onboard micro SD card socket (backside of the module). It is connected to SDHC2 of the NXP® i.MX 8M Plus processor. Four lanes are used for data. The micro SD card socket supports:

- OS boot
- U-Boot (Optional)
- SD/SDIO specification 3.0
- 200 MHz 1.8V signaling for up to 100 MBps
- Secure Digital eXtended Capacity (SDXC™) cards
- UHS-I (SDR104/50 and DDR50)
- Default Mode and High Speed Mode

6.9 RTC

The conga-QMX8-Plus offers a discrete Real-Time Clock (RTC) via an onboard MicroCrystal RV-4162-C7 module (I²C Address: 0xD0) with a time accuracy of ±20 ppm @ 25°C. This RTC module is powered via the Qseven® VCC_RTC rail or a 3.3V rail.

Note

The conga-QMX8-Plus has onboard Schottky diodes that prevent reverse current.

7 Signal Descriptions and Pinout Tables

Click on the screenshot below to directly download the conga-QMX8-Plus pinout as an Excel file:

QX8P Qseven edge connection								
QX8P / conga-QMX8-Plus Interface	i.MX8MP Ball Name	i.MX8MP Ball	Qseven Pin Name	Qseven Pin	I/O	PU/PD	Remark	alt. Function
GND			GND	1				
GND			GND	2				
Gigabit Ethernet			GBE_MDI3-	3	I/O-DIFF		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_MDI2-	4	I/O-DIFF		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_MDI3+	5	I/O-DIFF		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_MDI2+	6	I/O-DIFF		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_LINK100#	7	O		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_LINK1000#	8	O		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_MDI1-	9	I/O-DIFF		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_MDI0-	10	I/O-DIFF		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_MDI1+	11	I/O-DIFF		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_MDI0+	12	I/O-DIFF		Ethernet controller (AR8031), i.MX8MP:ENET_QOS	
Gigabit Ethernet			GBE_LINK#	13	O		Ethernet controller (AR8031), i.MX8MP:ENET_QOS, only LINK1000 and LINK100	
Gigabit Ethernet			GBE_ACT#	14	O		Ethernet controller (AR8031), i.MX8MP:ENET_QOS, LINK#/ACT	

Alternatively, you can find the conga-QMX8-Plus pinout by selecting it from the drop-down list at:

https://git.congatec.com/arm-nxp/imx8-family/doc/cgtimx8_pinlist/tree/master

The Qseven® signals are described in the Qseven® Specification 2.1 publicly available at:

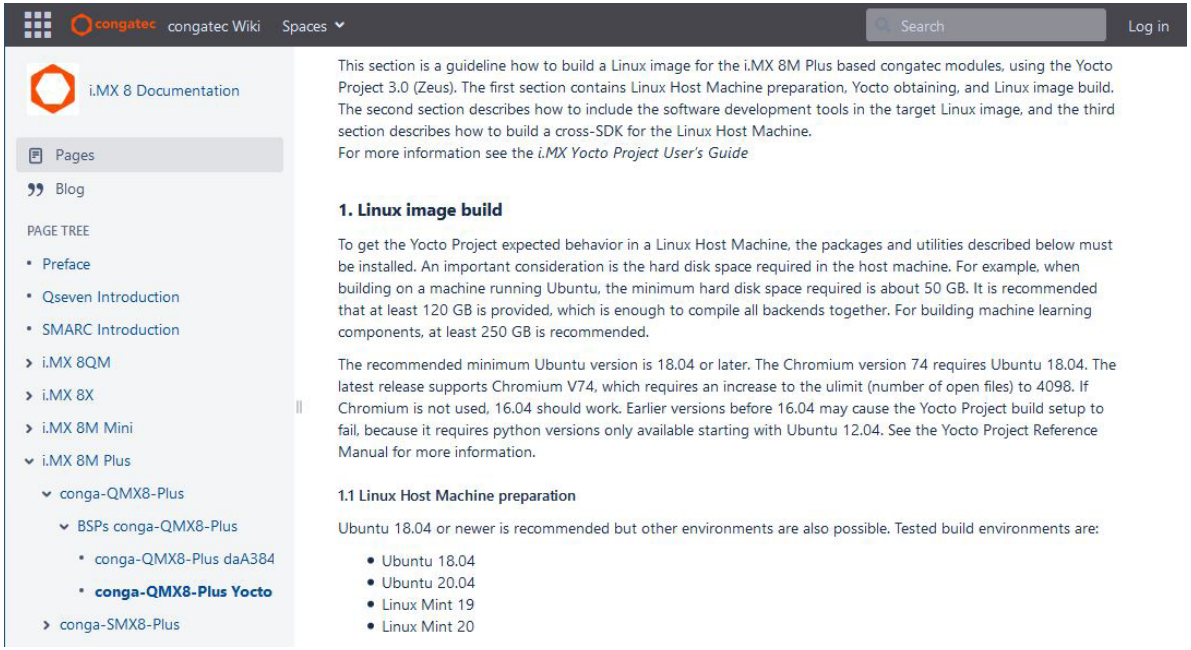
https://sget.org

The NXP® i.MX 8M Plus Applications Processor Datasheet for Commercial and Industrial Products is available at:

https://www.nxp.com

8 Software Documentation

Click on the screenshot below to open the conga-QMX8-Plus software documentation in your browser:



Alternatively, you can find the conga-QMX8-Plus software documentation by selecting it from the navigation menu at:

https://wiki.congatec.com

FORTEC
ELEKTRONIK AG

Our company network supports you worldwide with offices in Germany, Austria, Switzerland, the UK and the USA. For more information please contact:

Headquarters

Germany

FORTEC ELEKTRONIK AG

FORTEC Elektronik AG
Augsburger Str. 2b
82110 Germering

Phone: +49 89 894450-0
E-Mail: info@fortecag.de
Internet: www.fortecag.de

Fortec Group Members

Austria

DISTEC
A FORTEC GROUP MEMBER

Distec GmbH,
Office Vienna
Nuschinggasse 12
1230 Wien

Phone: +43 1 8673492-0
E-Mail: info@distec.de
Internet: www.distec.de

Germany

DISTEC
A FORTEC GROUP MEMBER

Distec GmbH
Augsburger Str. 2b
82110 Germering

Phone: +49 89 894363-0
E-Mail: info@distec.de
Internet: www.distec.de

Switzerland

ALTRAC
A FORTEC GROUP MEMBER

ALTRAC AG
Bahnhofstraße 3
5436 Würenlos

Phone: +41 44 7446111
E-Mail: info@altrac.ch
Internet: www.altrac.ch

United Kingdom

DISPLAY TECHNOLOGY
A FORTEC GROUP MEMBER

Display Technology Ltd.
Osprey House, 1 Osprey Court
Hinchingbrooke Business Park
Huntingdon, Cambridgeshire, PE29 6FN

Phone: +44 1480 411600
E-Mail: info@displaytechnology.co.uk
Internet: www. displaytechnology.co.uk

USA

APOLLO DISPLAY TECHNOLOGIES
A FORTEC GROUP MEMBER

Apollo Display Technologies, Corp.
87 Raynor Avenue,
Unit 1Ronkonkoma,
NY 11779

Phone: +1 631 5804360
E-Mail: info@apollodisplays.com
Internet: www.apollodisplays.com