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# Datasheet

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# Product Specification

AU OPTRONICS CORPORATION

( ) Preliminary Specifications

( V ) Final Specifications

<b>Module</b>	<b>17.3”(17.26”) UHD 16:9 Color TFT-LCD with LED Backlight design</b>
<b>Model Name</b>	B173ZAN01.0 (H/W:2A)
<b>Note</b> (  )	<b><i>LED Backlight with driving circuit design</i></b>

<b>Customer</b>	<b>Date</b>
<b>Checked &amp; Approved by</b>	<b>Date</b>
<p>Note: This Specification is subject to change without notice.</p>	

<b>Approved by</b>	<b>Date</b>
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# Product Specification

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## Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2015/05/12	All	First Edition for Customer		
0.2 2015/06/03	P28~P30	EDID update		
0.3 2015/06/24	P26		Shipping label	
0.4 2015/09/01	P6, P26		Gx, Gy, Shipping label	
0.5 2015/09/22	P26.P28~P30		Update EDID & label	
0.6 2015/11/17	P13 P26		Update Power Specification Update shipping label	

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## 1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

## 2. General Description

B173ZAN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:9 UHD, 3840(H) x2160(V) screen and 16.7M colors (RGB 8-bits data driver) with LED backlight driving circuit. All input signals are eDP(Embedded DisplayPort) interface compatible.

B173ZAN01.0 is designed for a display unit of notebook style personal computer and industrial machine.

### 2.1 General Specification

The following items are characteristics summary on the table at 25 °C condition:

Items	Unit	Specifications			
Screen Diagonal	[mm]	17.3"(17.26)			
Active Area	[mm]	382.12 x 214.94			
Pixels H x V		3840 x 3 (RGB) x 2160			
Pixel Pitch	[mm]	0.0995 x 0.0995			
Pixel Format		R.G.B. Vertical Stripe			
Display Mode		Normally Black			
White Luminance (I <sub>LED</sub> =TBDmA) (Note: I <sub>LED</sub> is LED current)	[cd/m <sup>2</sup> ]	400 typ. (5 points average) 340 min. (5 points average)			
Luminance Uniformity		1.25 max. (5 points)			
Contrast Ratio		1000 typ			
Response Time	[ms]	30 max.			
Nominal Input Voltage VDD	[Volt]	+3.3 typ.			
Power Consumption	[Watt]	14.0 (Include Logic and Blu power)			
Weight	[Grams]	550 max.			
Physical Size Include bracket	[mm]		Min.	Typ.	Max.
		Length	397.60	398.10	398.60
		Width	245.60	246.10	246.60
		Thickness	-	-	4
Electrical Interface		4 Lane eDP 1.3			
Glass Thickness	[mm]	0.5			
Surface Treatment		Anti-Glare, Hardness 3H			
Support Color		16.7M colors ( RGB 8-bit )			

Temperature Range Operating	[°C]	0 to +50
Storage (Non-Operating)	[°C]	-20 to +60
RoHS Compliance		RoHS Compliance

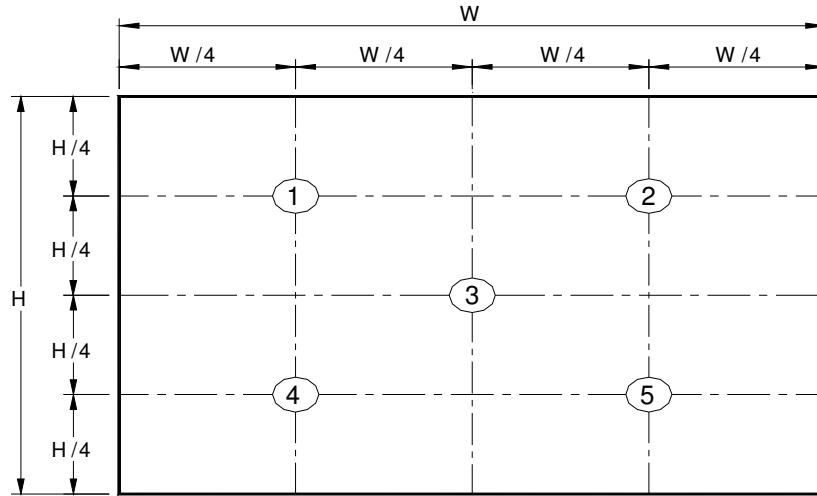
## 2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature) :

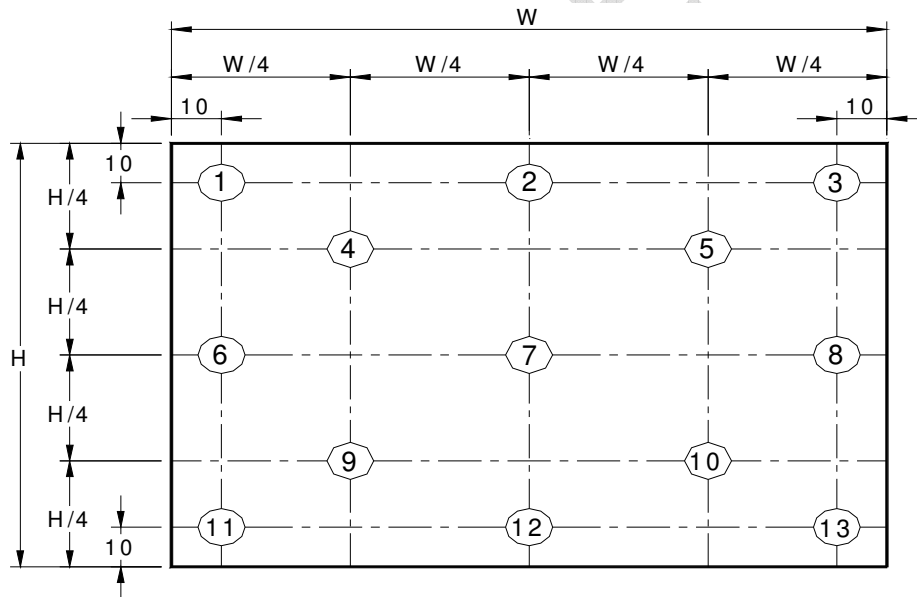
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
White Luminance $I_{LED}=20mA$		5 points average	340	400	-	cd/m <sup>2</sup>	1, 4, 5.
Viewing Angle	$\theta_R$	Horizontal (Right) CR = 10 (Left)	85	89	-	degree	4, 9
	$\theta_L$		85	89	-		
	$\phi_H$	Vertical (Upper) CR = 10 (Lower)	85	89	-		
	$\phi_L$		85	89	-		
Luminance Uniformity	$\delta_{5P}$	5 Points	-	-	1.25		1, 3, 4
Luminance Uniformity	$\delta_{13P}$	13 Points	-	-	1.60		2, 3, 4
Contrast Ratio	CR		-	1000	-		4, 6
Cross talk	%				4		4, 7
Response Time	$T_{RT}$	Rising + Falling	-	27	30	msec	4, 8
Color / Chromaticity Coodinates	Red	Rx	CIE 1931	0.626	0.656	0.686	4
		Ry		0.284	0.314	0.344	
	Green	Gx		0.182	0.212	0.242	
		Gy		0.681	0.711	0.741	
	Blue	Bx		0.118	0.148	0.178	
		By		0.027	0.057	0.087	
	White	Wx		0.283	0.313	0.343	
		Wy		0.299	0.329	0.359	
	Adobe	%			-	100	



**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

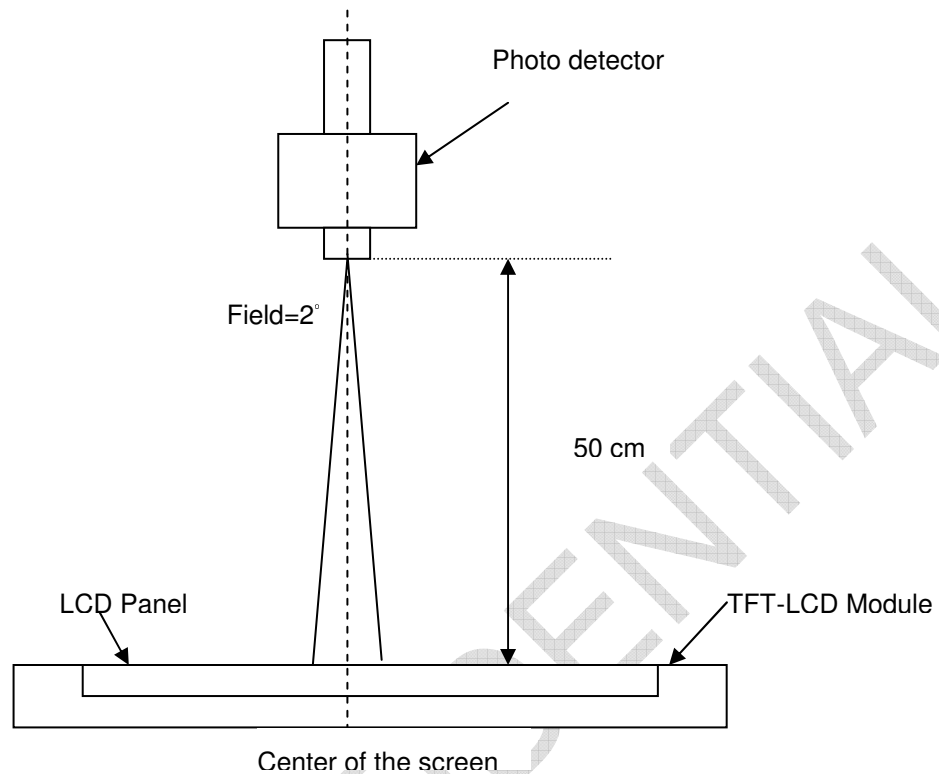
$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4:** Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting

Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



**Note 5 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ·  $Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$

$L (x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

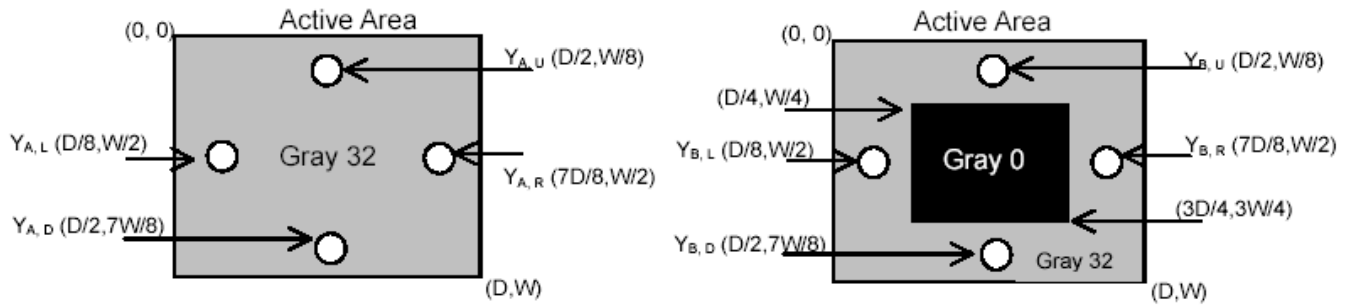
**Note 7 :** Definition of Cross Talk (CT)

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where

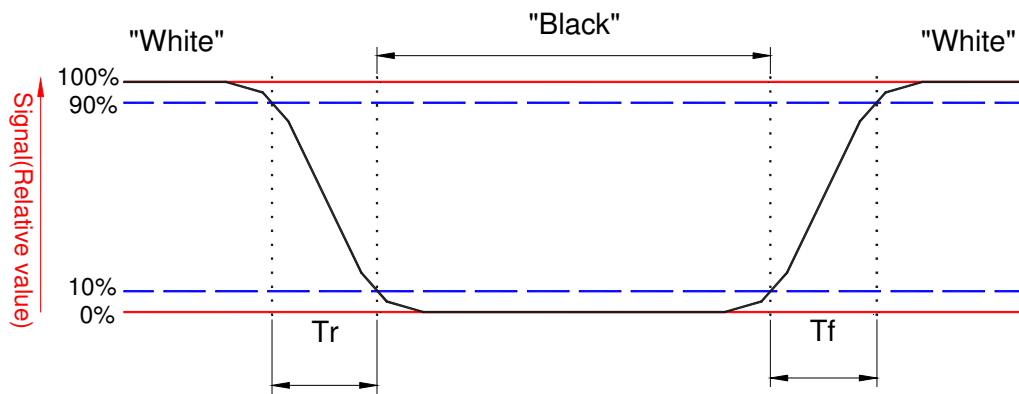
$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



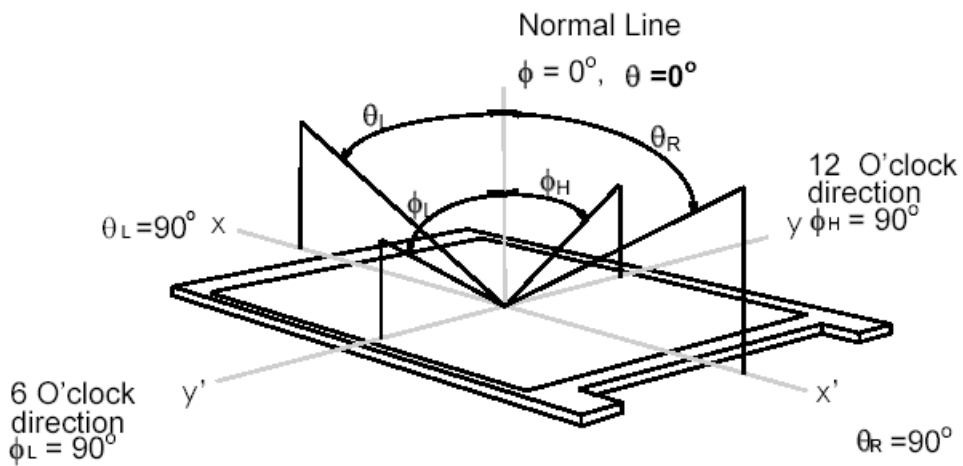
**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from “White” to “Black” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



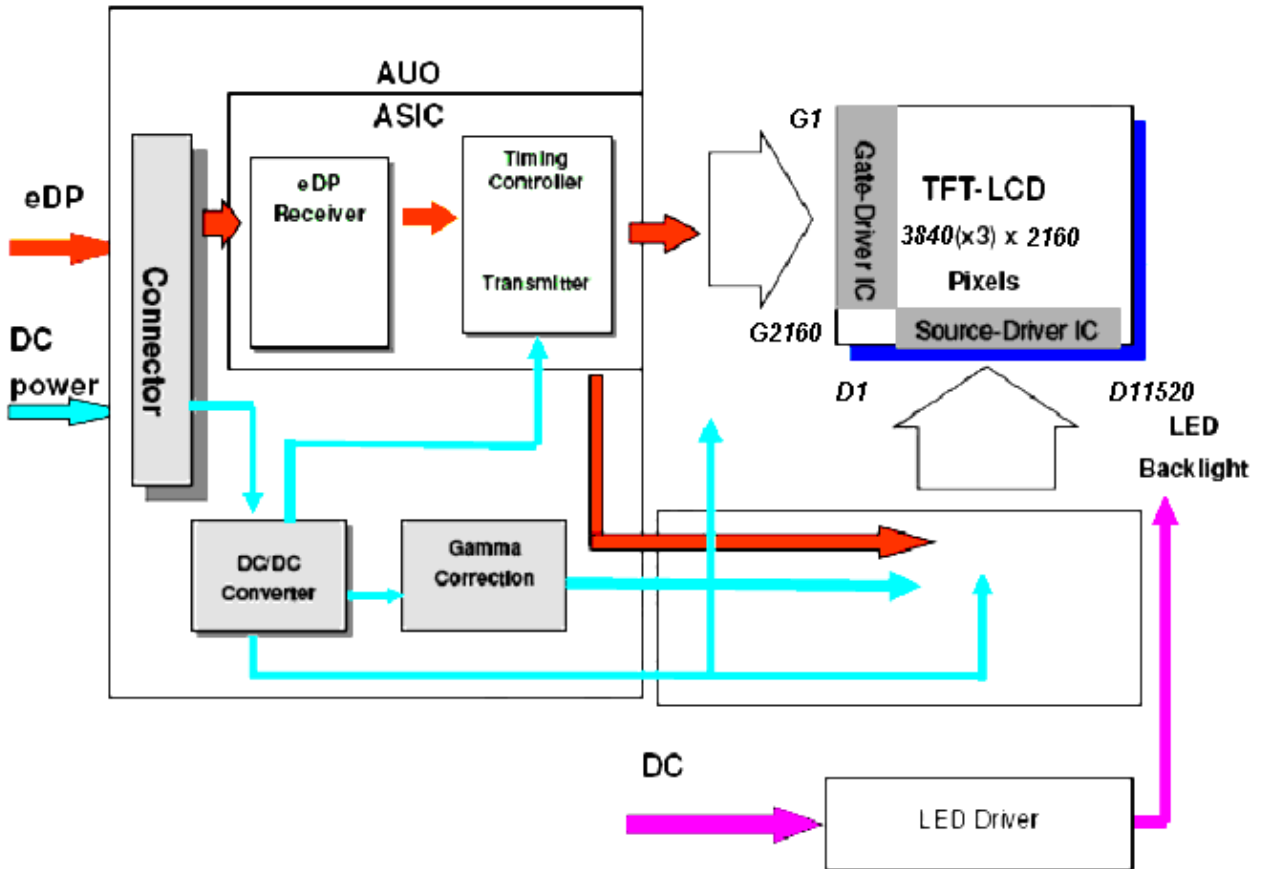
**Note 9.** Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



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## 3. Functional Block Diagram



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## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	Vin	-0.3	+4.0	[Volt]	Note 1,2

### 4.2 Absolute Ratings of Environment

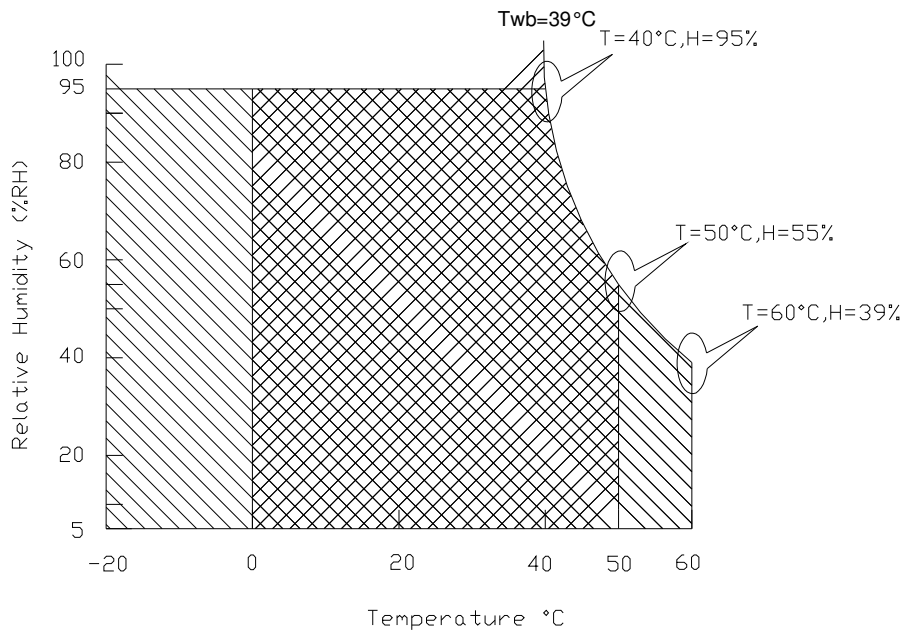
Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 4
Operation Humidity	HOP	5	95	[%RH]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4
Storage Humidity	HST	5	95	[%RH]	Note 4

Note 1: At Ta (25°C )

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range

Storage Range +

## 5. Electrical Characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

Input power specifications are as follows;

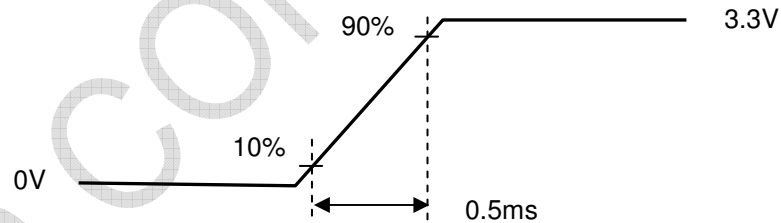
The power specification are measured under 25°C and frame frequency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	2.5	[Watt]	Note 1
IDD	IDD Current	-	-	833	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition : Black Pattern at 3.3V driving voltage. ( $P_{max}=V_{3.3} \times I_{black}$ )

Typical Measurement Condition : Mosaic Pattern

Note 2 : Measure Condition



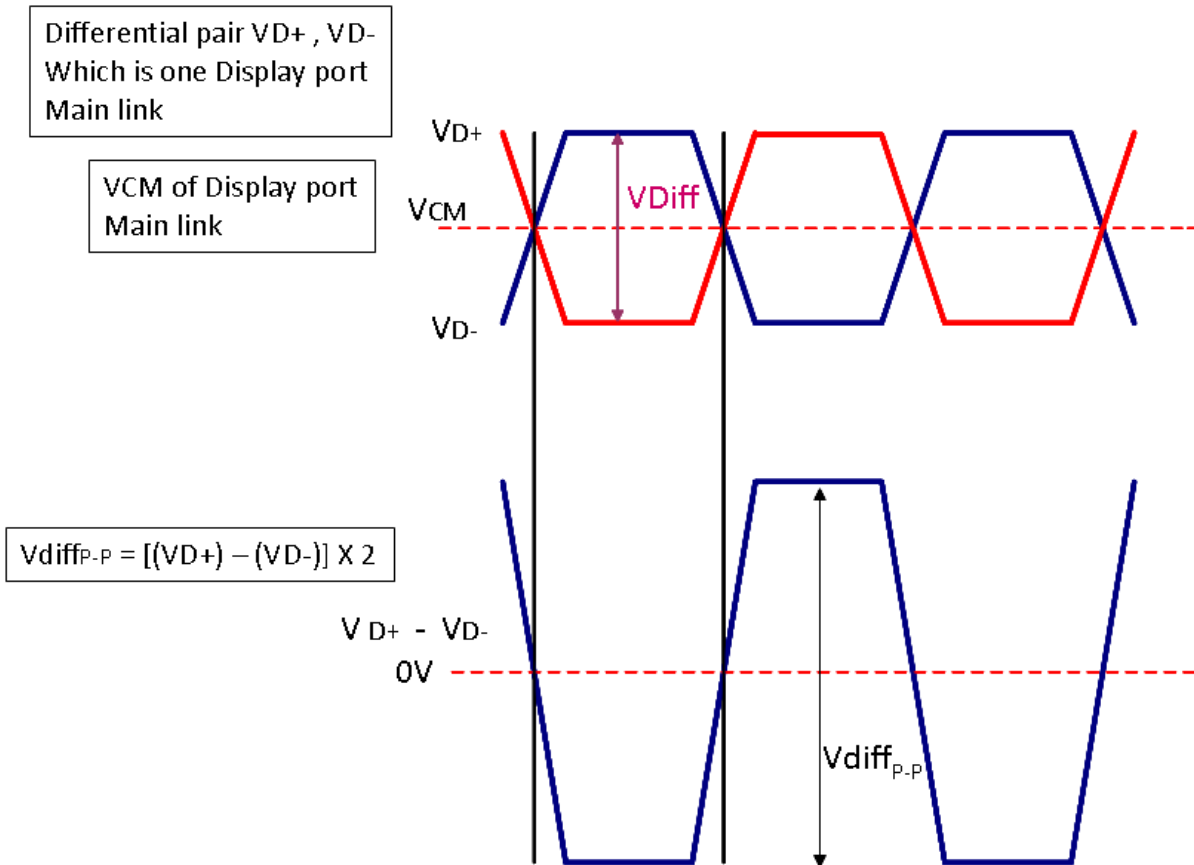
Vin rising time

## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Signal electrical characteristics are as follows;

### Display Port main link signal:



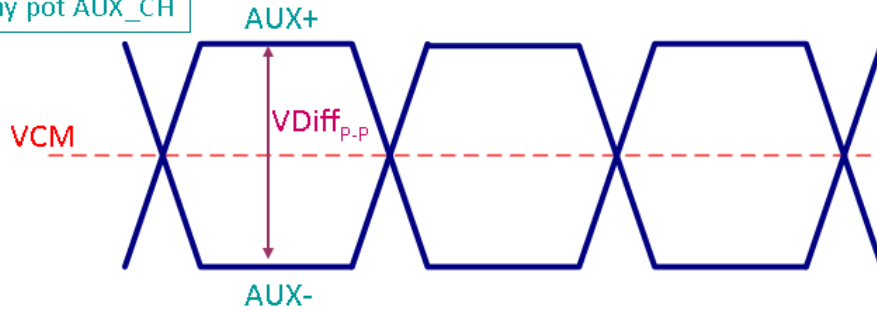
Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
VDiff <sub>P-P</sub>	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Follow as VESA display port standard V1.



## Display Port AUX\_CH signal:

Differential AUX+ , AUX-  
Which is Display port AUX\_CH



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff <sub>p-p</sub>	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Fallow as VESA display port standard V1.1a.

## Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2		3.6	V

Fallow as VESA display port standard V1.1a.

## 5.2 Backlight Unit

### 5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	RG phosphor	-	-	10	[Watt]	(Ta=25°C), Note 1 Vin =12V
LED Life-Time	N/A	-	15,000	-	Hour	(Ta=25°C), Note 2 If=TBD mA

**Note 1:** Calculator value for reference  $P_{LED} = VF$  (Normal Distribution) \*  $I_F$  (Normal Distribution) / Efficiency

**Note 2:** The LED life-time define as the estimated time to 50% degradation of initial luminous.

### 5.2.2 Backlight input signal characteristics

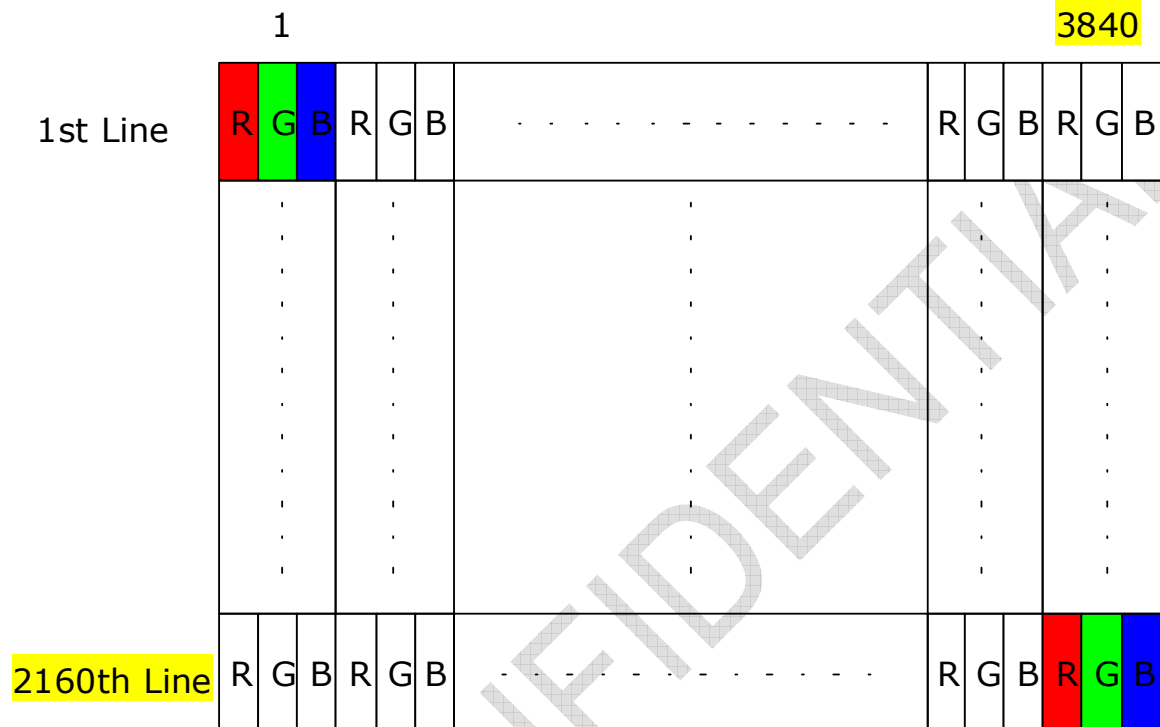
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	10	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25°C)
LED Enable Input High Level	VLED_EN	2.5	-	3.3	[Volt]	
LED Enable Input Low Level		-	-	0.5	[Volt]	
PWM Logic Input High Level	VPWM_EN	2.5	-	3.3	[Volt]	
PWM Logic Input Low Level		-	-	0.5	[Volt]	
PWM Input Frequency	FPWM	200	--	10K	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

**Note 1 :** Recommend system pull up/down resistor no bigger than 10kohm

## 6. Signal Interface Characteristic

### 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



## 6.2 Integration Interface Requirement

### 6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	I-PEX or compatible
Type / Part Number	eDP / 20455-040E-12R or compatible
Mating Housing/Part Number	I-PEX / 20453-040T-01 or compatible

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## 6.2.2 Pin Assignment

Model		
Pin	Signal Name	Description
1	NC	No Connect (Reserved for DCR)
2	H_GND	High Speed Ground
3	Lane3_N	Comp Signal Lane3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Comp Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Comp Signal Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Comp Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Ch.
16	AUX_CH_N	Comp Signal Auxiliary Ch.
17	H_GND	High Speed Ground
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	LCD_Self_Test	LCD Panel Self Test Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight_ground
29	BL_GND	Backlight_ground
30	BL_GND	Backlight_ground
31	BL_GND	Backlight_ground
32	BL_Enable	Backlight On / Off
33	BL_PWM_DIM	System PWM signal Input
34	H_SYNC or NC	H_SYNC function (Optional) or NC
35	NC	NC
36	BL_PWR	Backlight power (10V~21V)
37	BL_PWR	Backlight power (10V~21V)
38	BL_PWR	Backlight power (10V~21V)
39	BL_PWR	Backlight power (10V~21V)
40	NC	No Connect (Reserved for CM)

## 6.3 Interface Timing

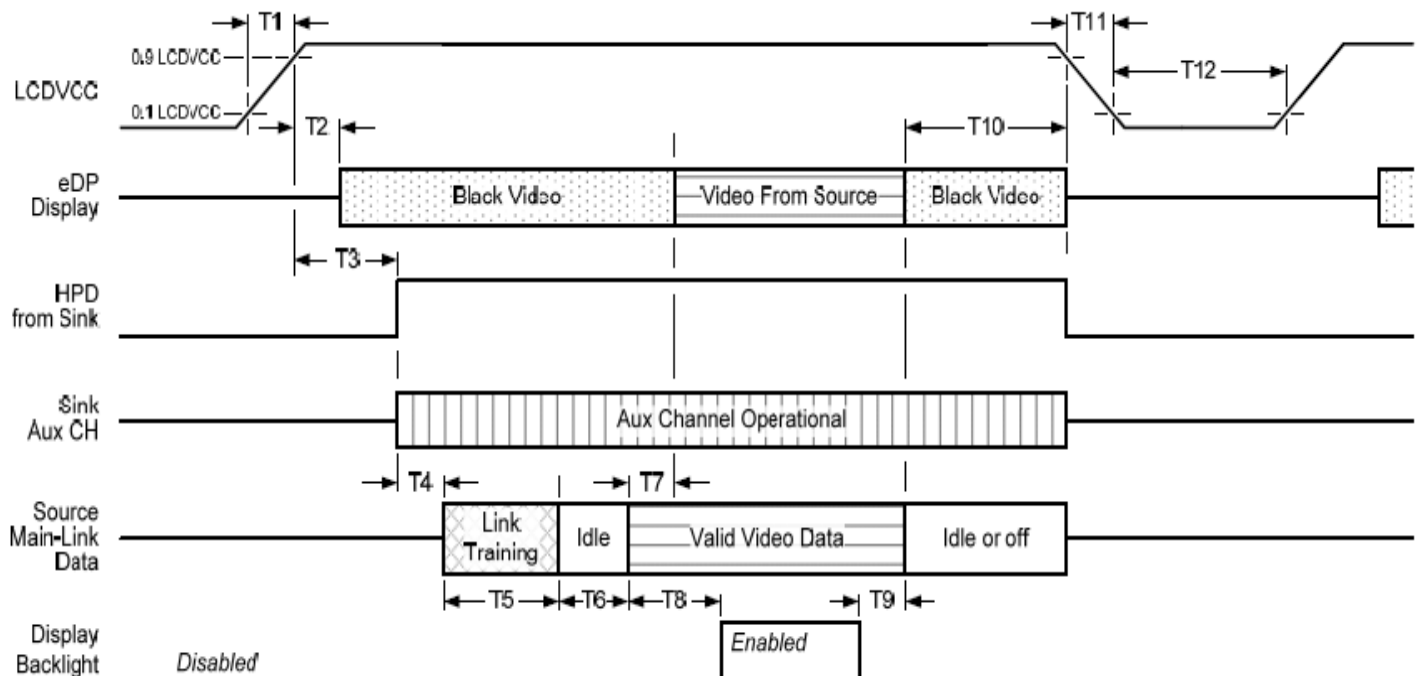
### 6.3.1 Timing Characteristics

Basically, interface timings should match the 3840x2160 /60Hz manufacturing guide line timing.

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Frame Rate	-	-	60	-	Hz	
Clock frequency	$1/T_{Clock}$	.	533.5	.	MHz	
Vertical Section	Period	$T_V$	.	2222	.	$T_{Line}$
	Active	$T_{VD}$	2160			
	Blanking	$T_{VB}$	.	62	.	
Horizontal Section	Period	$T_H$	.	4000	.	$T_{Clock}$
	Active	$T_{HD}$	3840			
	Blanking	$T_{HB}$	.	160	.	

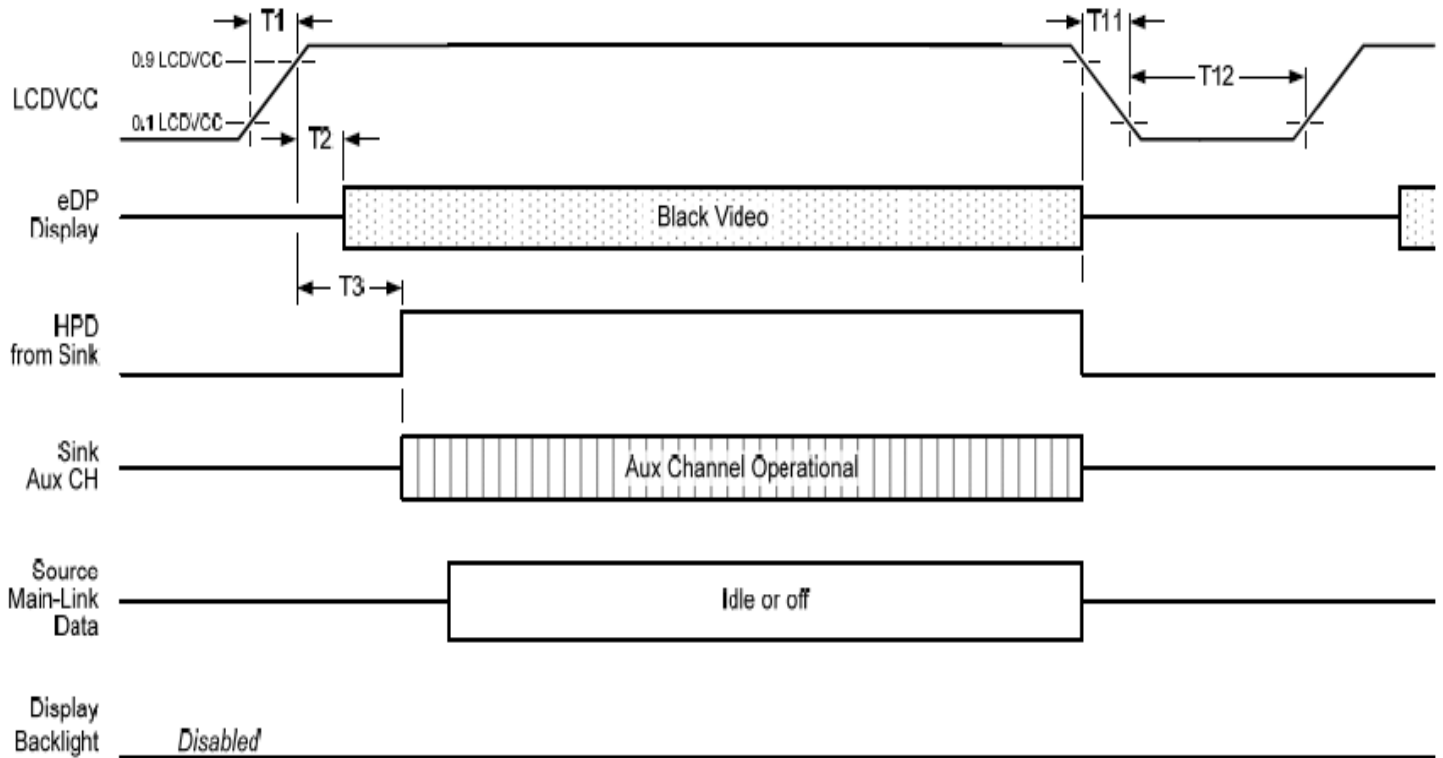
## 6.4 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX\_CH transaction only:



**Display port interface power up/down sequence, AUX\_CH transaction only**

**Display Port panel power sequence timing parameter:**

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

**Note1:** The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

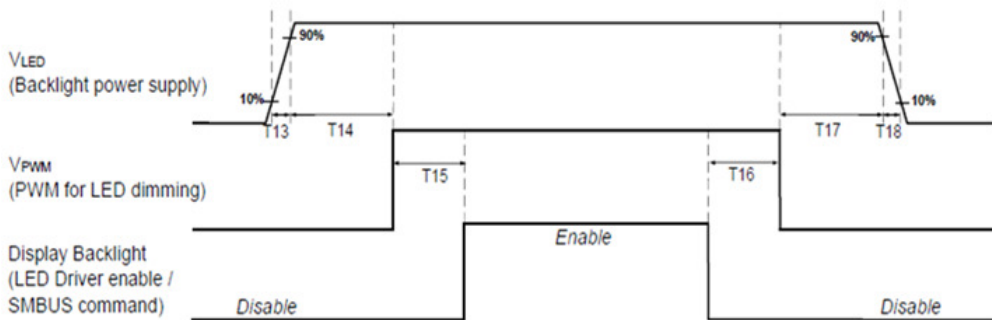
- upon LCDVDD power on (with in T2 max)-when the "Novideostream\_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

- when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

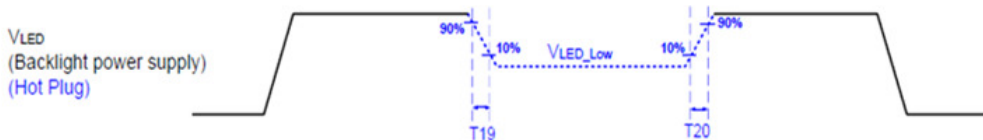
**Note 2:** The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

**Note 3:** The sink must support AUX\_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX\_CH transaction with the time specified within T3 max.

## Display Port panel B/L power sequence timing parameter:



Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change:  $T19/T20 = 5 \times T_{PWM}^*$

\* $T_{PWM} = 1/PWM \text{ Frequency}$



## 7. Panel Reliability Test

### 7.1 Vibration Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test

**Test Spec:**

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3 Reliability Test

Items	Required Condition	Note
Temperature Humidity Bias	Ta= 40°C, 90%RH, 300h	
High Temperature Operation	Ta= 50°C, Dry, 300h	
Low Temperature Operation	Ta= 0°C, 300h	
High Temperature Storage	Ta= 60°C, 35%RH, 300h	
Low Temperature Storage	Ta= -20°C, 50%RH, 250h	
Thermal Shock Test	Ta=-20°C to 60°C, Duration at 30 min, 100 cycles	
ESD	Contact : ±8 KV Air : ±15 KV	Note 1

**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. Self-recoverable.  
No data lost, No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%

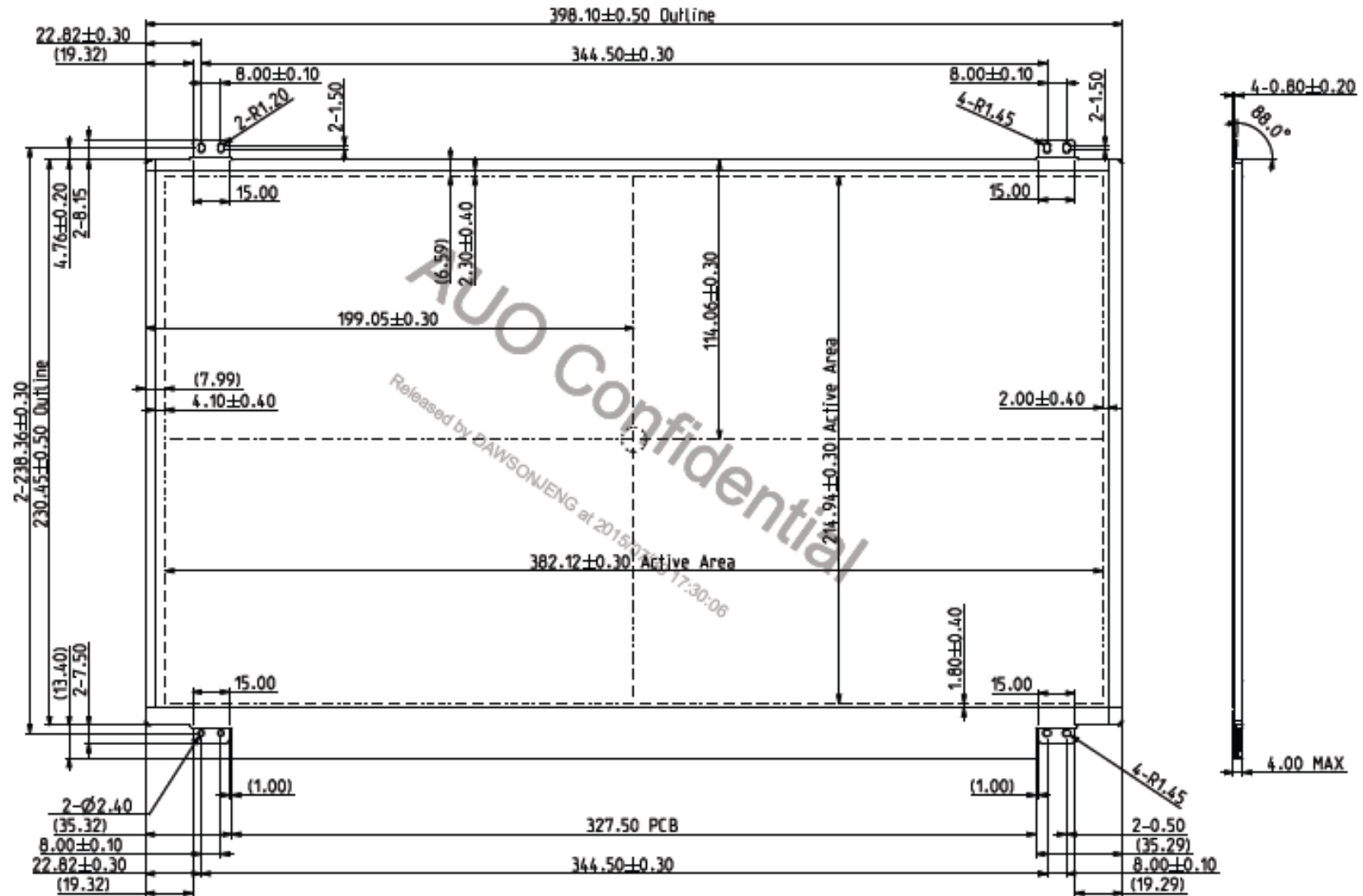


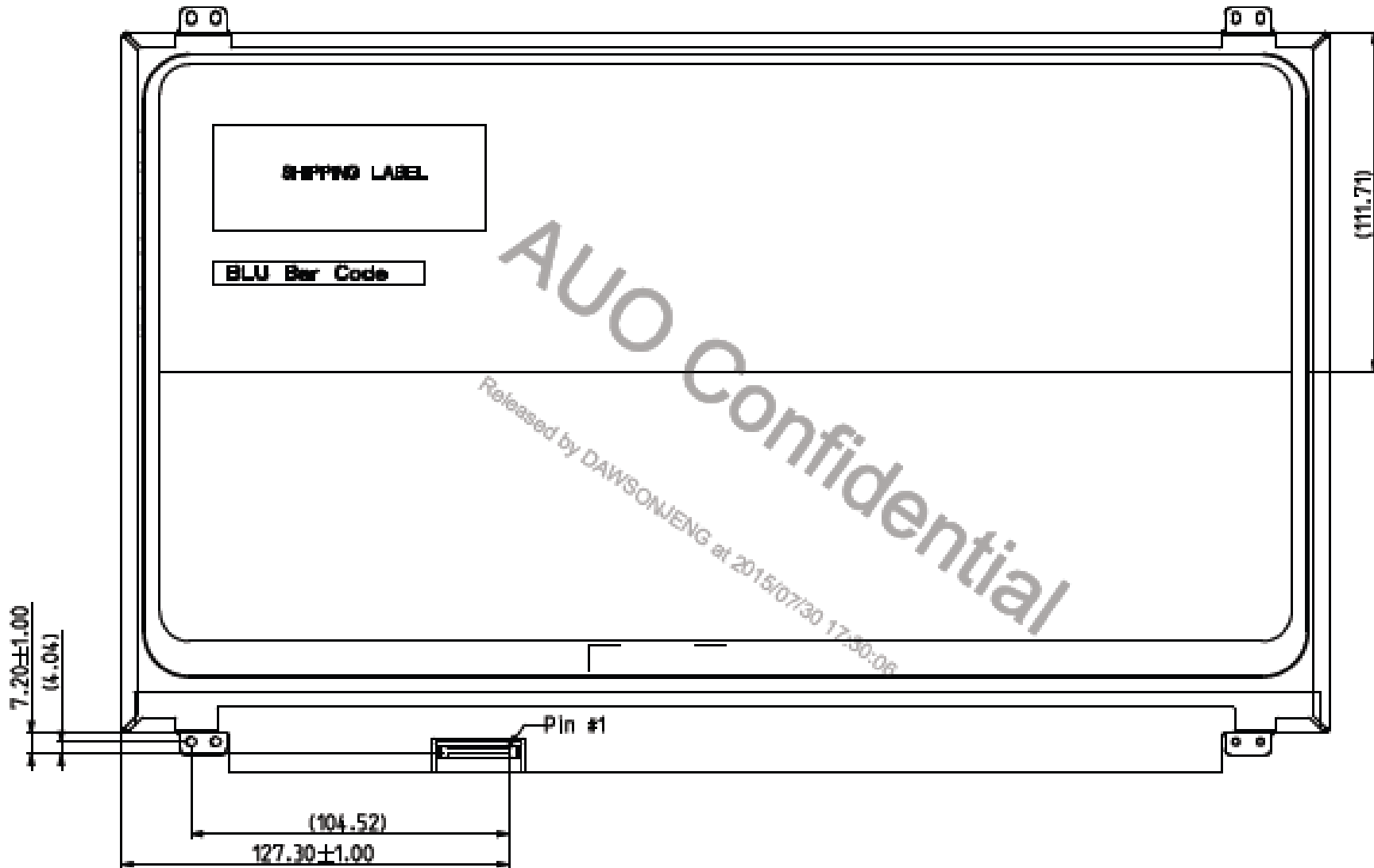
# Product Specification

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## 8. Mechanical Characteristics

### 8.1 LCM Outline Dimension

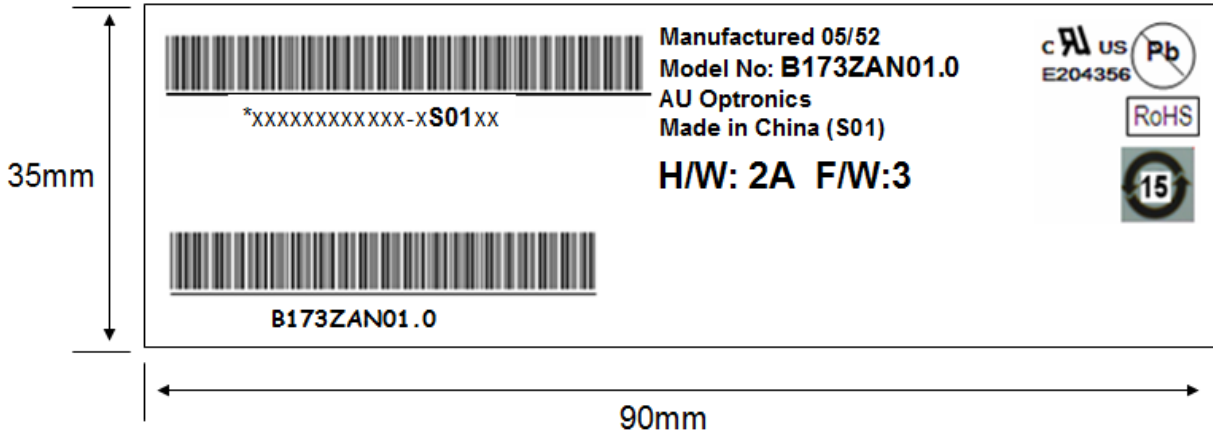




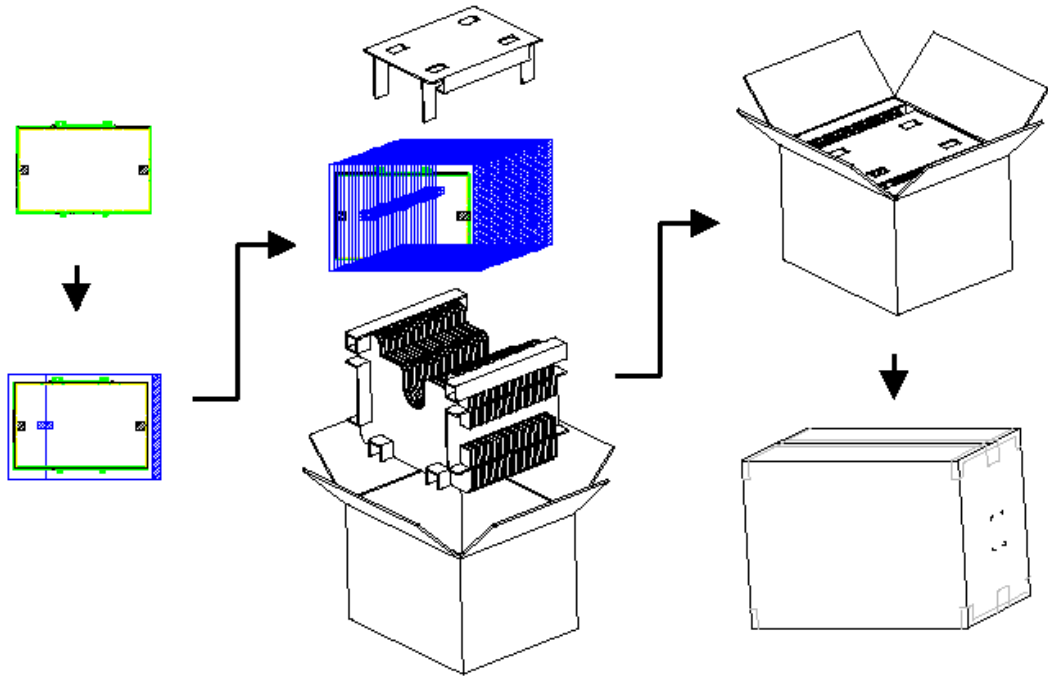
Note: Prevention IC damage, IC positions not allowed any overlap over these areas.

## 9. Shipping and Package

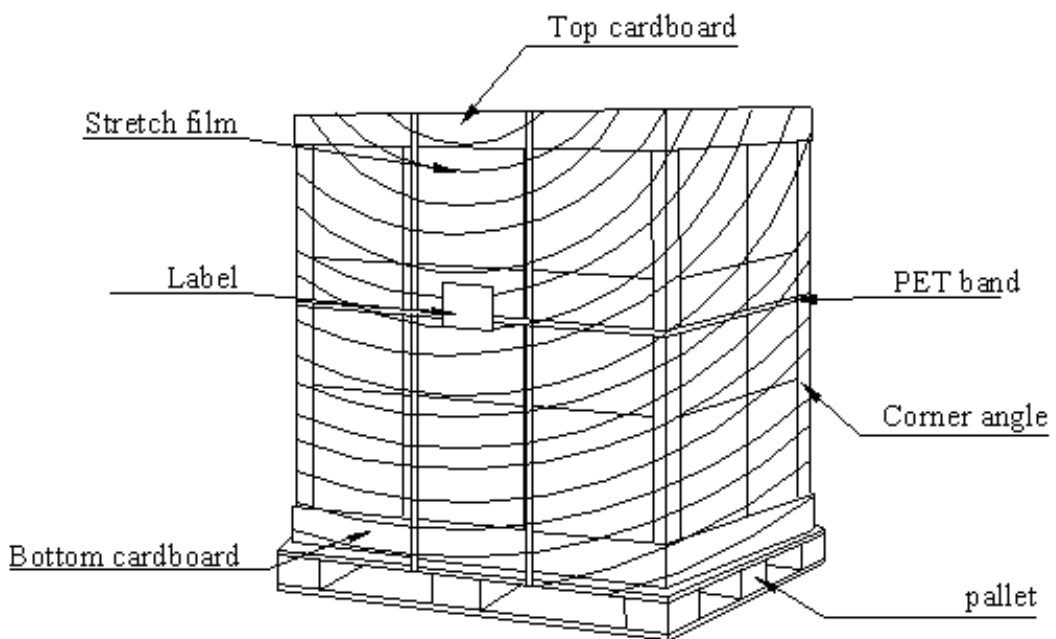
### 9.1 Shipping Label Format



AL



### 9.3 Shipping Package of Palletizing Sequence





# Product Specification

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## 10. Appendix: EDID Description

Address	FUNCTION	Value	Value	Value
HEX		HEX	BIN	DEC
00	Header	00	00000000	0
01		FF	11111111	255
02		FF	11111111	255
03		FF	11111111	255
04		FF	11111111	255
05		FF	11111111	255
06		FF	11111111	255
07		00	00000000	0
08	EISA Manuf. Code LSB	06	00000110	6
09	Compressed ASCII	AF	10101111	175
0A	Product Code	9B	10011011	155
0B	hex, LSB first	10	00010000	16
0C	32-bit ser #	00	00000000	0
0D		00	00000000	0
0E		00	00000000	0
0F		00	00000000	0
10	Week of manufacture	00	00000000	0
11	Year of manufacture	19	00011001	25
12	EDID Structure Ver.	01	00000001	1
13	EDID revision #	04	00000100	4
14	<b>Video input def.</b> ( <i>digital I/P, non-TMDS, CRGB</i> )	A5	10100101	165
15	<b>Max H image size</b> ( <i>rounded to cm</i> )	26	00100110	38
16	<b>Max V image size</b> ( <i>rounded to cm</i> )	15	00010101	21
17	<b>Display Gamma</b> ( <i>=(gamma*100)-100</i> )	78	01111000	120
18	<b>Feature support</b> ( <i>no DPMS, Active OFF, RGB, tmg Blk#1</i> )	02	00000010	2
19	Red/green low bits ( <b>Lower 2:2:2:2 bits</b> )	24	00100100	36
1A	Blue/white low bits ( <b>Lower 2:2:2:2 bits</b> )	25	00100101	37
1B	Red x ( <b>Upper 8 bits</b> )	A8	10101000	168
1C	Red y/ highER 8 bits	50	01010000	80
1D	Green x	36	00110110	54
1E	Green y	B6	10110110	182
1F	Blue x	26	00100110	38
20	Blue y	0E	00001110	14
21	White x	50	01010000	80
22	White y	54	01010100	84
23	Established timing 1	00	00000000	0
24	Established timing 2	00	00000000	0
25	Established timing 3	00	00000000	0
26	Standard timing #1	01	00000001	1
27		01	00000001	1
28	Standard timing #2	01	00000001	1
29		01	00000001	1
2A	Standard timing #3	01	00000001	1
2B		01	00000001	1



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2C	Standard timing #4	01	00000001	1
2D		01	00000001	1
2E	Standard timing #5	01	00000001	1
2F		01	00000001	1
30	Standard timing #6	01	00000001	1
31		01	00000001	1
32	Standard timing #7	01	00000001	1
33		01	00000001	1
34	Standard timing #8	01	00000001	1
35		01	00000001	1
36	Pixel Clock/10000 LSB	66	01100110	102
37	Pixel Clock/10000 USB	D0	11010000	208
38	Horz active <b>Lower 8bits</b>	00	00000000	0
39	Horz blanking <b>Lower 8bits</b>	A0	10100000	160
3A	HorzAct:HorzBlnk <b>Upper 4:4 bits</b>	F0	11110000	240
3B	Vertical Active <b>Lower 8bits</b>	70	01110000	112
3C	Vertical Blanking <b>Lower 8bits</b>	3E	00111110	62
3D	Vert Act : Vertical Blanking <b>(upper 4:4 bit)</b>	80	10000000	128
3E	HorzSync. Offset	30	00110000	48
3F	HorzSync.Width	20	00100000	32
40	VertSync.Offset : VertSync.Width	35	00110101	53
41	Horz&Vert Sync Offset/Width <b>Upper 2bits</b>	00	00000000	0
42	Horizontal Image Size <b>Lower 8bits</b>	7E	01111110	126
43	Vertical Image Size <b>Lower 8bits</b>	D6	11010110	214
44	Horizontal & Vertical Image Size <b>(upper 4:4 bits)</b>	10	00010000	16
45	Horizontal Border <i>(zero for internal LCD)</i>	00	00000000	0
46	Vertical Border <i>(zero for internal LCD)</i>	00	00000000	0
47	Signal <i>(non-intr, norm, no stero, sep sync, neg pol)</i>	18	00011000	24
48	Detailed timing/monitor	00	00000000	0
49	descriptor #2	00	00000000	0
4A		00	00000000	0
4B		0F	00001111	15
4C		00	00000000	0
4D		00	00000000	0
4E		00	00000000	0
4F		00	00000000	0
50		00	00000000	0
51		00	00000000	0
52		00	00000000	0
53		00	00000000	0
54		00	00000000	0
55		00	00000000	0
56		00	00000000	0
57		00	00000000	0
58		00	00000000	0
59		20	00100000	32
5A	Detailed timing/monitor	00	00000000	0



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5B	descriptor #3	00	00000000	0
5C		00	00000000	0
5D		FE	11111110	254
5E		00	00000000	0
5F	Manufacture	41	01000001	65
60	Manufacture	55	01010101	85
61	Manufacture	4F	01001111	79
62		0A	00001010	10
63		20	00100000	32
64		20	00100000	32
65		20	00100000	32
66		20	00100000	32
67		20	00100000	32
68		20	00100000	32
69		20	00100000	32
6A		20	00100000	32
6B		20	00100000	32
6C	Detailed timing/monitor	00	00000000	0
6D	descriptor #4	00	00000000	0
6E		00	00000000	0
6F		FE	11111110	254
70		00	00000000	0
71	Manufacture P/N	42	01000010	66
72	Manufacture P/N	31	00110001	49
73	Manufacture P/N	37	00110111	55
74	Manufacture P/N	33	00110011	51
75	Manufacture P/N	5A	01011010	90
76	Manufacture P/N	41	01000001	65
77	Manufacture P/N	4E	01001110	78
78	Manufacture P/N	30	00110000	48
79	Manufacture P/N	31	00110001	49
7A	Manufacture P/N	2E	00101110	46
7B	Manufacture P/N	30	00110000	48
7C		20	00100000	32
7D		0A	00001010	10
7E	Extension Flag	00	00000000	0
7F	Checksum	3B	00111011	59



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