FORTEC
GROUP

Datasheet

InnoLux

S850DJJ-T05

CH-01-081

FORTEC
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☐ Tentative Specification
■ Preliminary Specification
☐ Approval Specification

MODEL NO.: S850DJJ

SUFFIX: T05

Revision:
Customer:

APPROVED BY SIGNATURE

Name / Title _____ _____
Note

_____
Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chris Chen	John Hsieh	Chiawen Chen

CONTENTS

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 1.1	Jul.4, 2024	All	All	The preliminary spec was first released

1. GENERAL DESCRIPTION

1.1 OVERVIEW

S850DJJ-T05 is a 84.5″ TFT Liquid Crystal Display PID module with LED Backlight unit and 8Lanes V-by-One HS interface. This module supports 3840 x 2160 Quad Full HDTV format and can display true 1.07G colors (8-bit+FRC). The converter module for backlight is built-in.

1.2 FEATURES

- High brightness 2500nits
- High contrast ratio 5000:1
- Fast response time Gray to Gray typical : 11 ms
- High color saturation NTSC 72%
- Quad Full HDTV (3840 x 2160 pixels) resolution, true HDTV format
- V-by-One HS interface
- Optimized response time for 50Hz/60Hz frame rate
- Viewing Angle : 178(H)/178(V) (CR>10) VA Technology
- Ultra wide viewing angle : Super MVA technology
- RoHs compliance
- T-con input frame rate * QFHD 47~63Hz
  Output frame rate: QFHD 47~63Hz

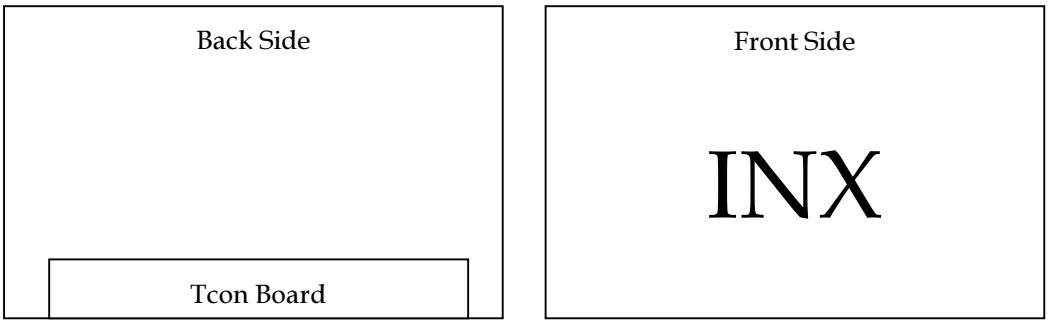
1.3 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1872(H)*1053(V) (85″ diagonal)	mm	(1)
Bezel Opening Area	1876(H)*1057(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840 x R.G.B. x 2160	pixel	-
Pixel Pitch (Sub Pixel)	0.1625 (H) x 0.4875 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G colors (8-bit+FRC)	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	AG (haze~28%), Hardness=3H	-	(2)
Rotation Function	Unachievable		(3)
Display Orientation	Signal input with “INX”		(3)
Remark	7*24Hrs Continuous Operation(dynamic video） Horizontal and Perpendicular Compatibility	-	-

Note (1) Please refer to the attached drawings in chapter 11 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. INX reserves the rights to change this feature.

Note (3)



1.4 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	1908.7	1910.8	1912.9	mm	(1),(2)
	Vertical (V)	1089.7	1091.8	1092.9	mm	(1),(2)
	Depth (D)	26.5	27.5	28.5	mm	To Rear
		48.1	49.1	50.1	mm	To CNV cover
Weight		(53000)			g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	60	ºC	(1), (3)
Operating Ambient Temperature	T_{OP}	-20	60	ºC	(1), (3)
Panel Surface Temperature	T_{PS}	-	+70	ºC	(2)

Note (1) Temperature and relative humidity range is shown in the figure below.

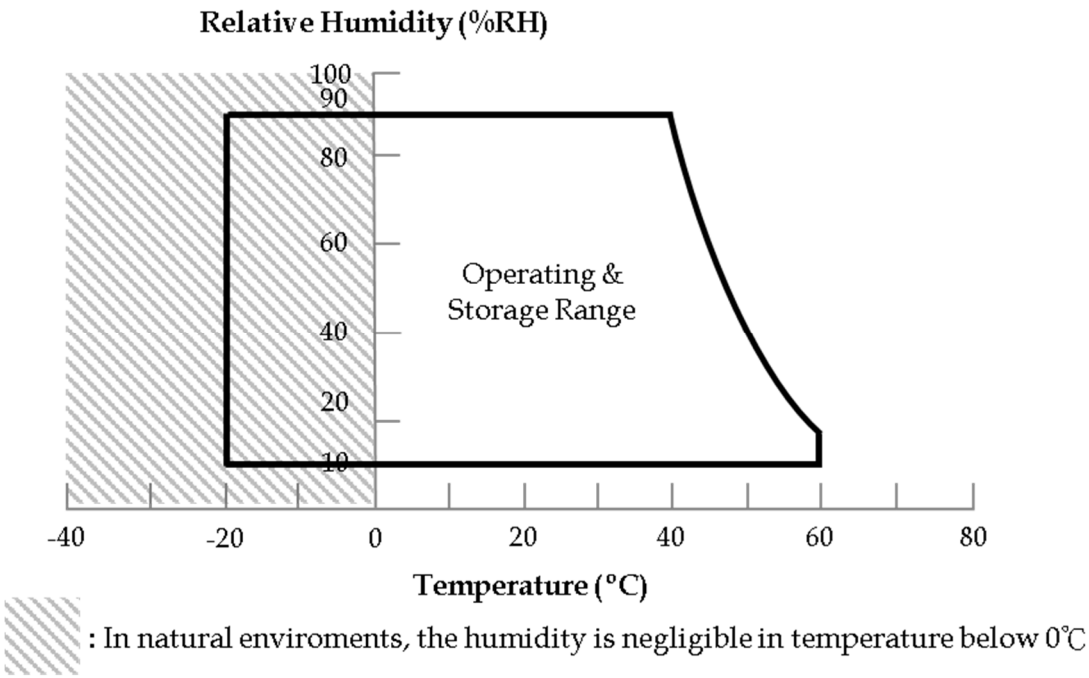
(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max.

(c) No condensation.

Note (2) Surface temperature is measured at 60℃ Dry condition.

Note (3) The rating of environment is based on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Light Bar Voltage	VW	—	60	VRMS	
Converter Input Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	6	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

3. ELECTRICAL CHARACTERISTICS

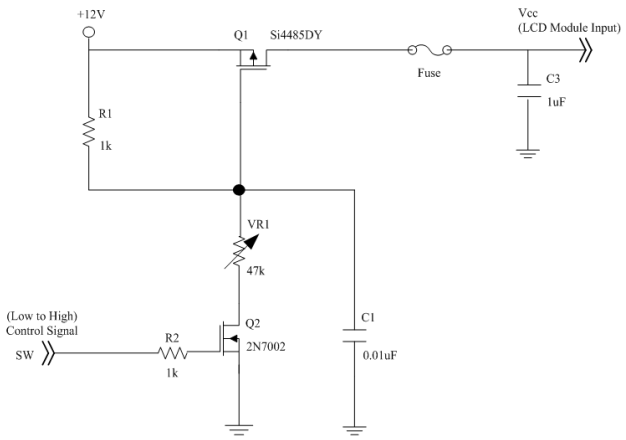
3.1 TFT LCD MODULE

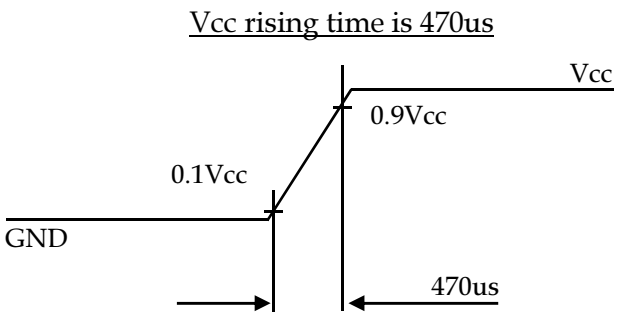
(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	(5.33)	A	(2)
Power Consumption	White Pattern	P_T	—	(37.95)	(41.745)	W	(3)
	Black Pattern	P_T	—	(15.787)	(17.367)	W	
	Horizontal Stripe	P_T	—	(37.536)	(41.29)	W	
Power Supply Current	White Pattern	—	—	(3.648)	(3.952)	A	(3)
	Black Pattern	—	—	(1.512)	(1.638)	A	
	Horizontal Stripe	—	—	(3.6)	(3.9)	A	
VbyOne HS	Differential Input High Threshold Voltage	VLVTH			+50	mV	
	Differential Input Low Threshold Voltage	VLVTL	-50			mV	
	Differential Input Resistor	RRIN	80	100	120	ohm	
CMOS interface	Input High Threshold Voltage	VIH	2.7		3.6	V	
	Input Low Threshold Voltage	VIL	0		0.7	V	

Note (1) The module should be always operated within the above ranges. The ripple voltage should be controlled under 10% of Vcc (Typ.)

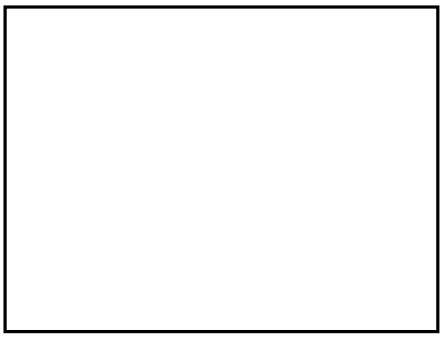
Note (2) Measurement condition :





Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, fv = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

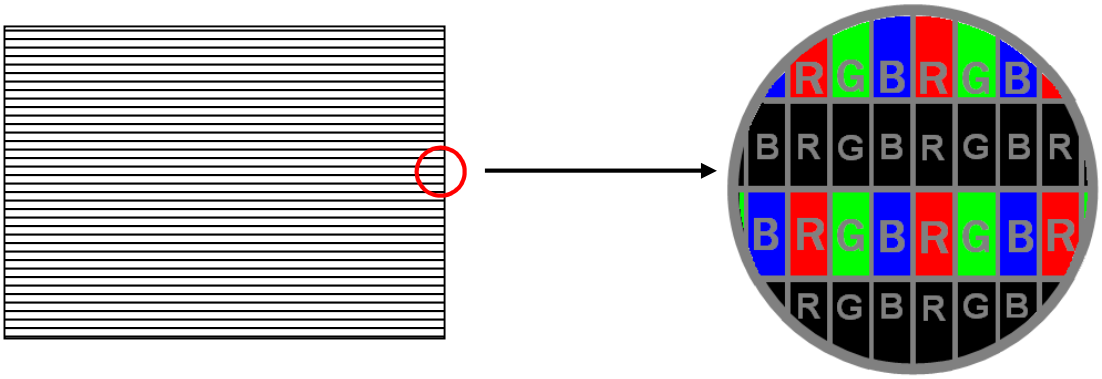


Active Area

b. Black Pattern

Active Area

c. Horizontal Stripe



3.2 BACKLIGHT CONVERTER UNIT

3.2.1 CONVERTER CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Power Consumption	P_{CNV}	-	(732)	(834)	W	(1), (2)
Each converter spec, This module uses 6 converter						
Power Consumption	P_{BL}		(122)	(139)		(1)
Converter Input Voltage	VBL	22.8	24.0	25.2	VDC	
Converter Input Current	I_{BL}	-	(5.1)	(5.8)	A	Non Dimming
Input Inrush Current	I_R	-	-	(10)	Apeak	V_{BL}=22.8V, (3) (6)
Dimming Frequency	FB	150	160	170	Hz	(5)
Dimming Duty Ratio	DDR	5	-	100	%	(4) (5)
Life Time	-	30,000	50,000	-	Hrs	(7)

Note (1) The power supply capacity should be higher than the total converter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

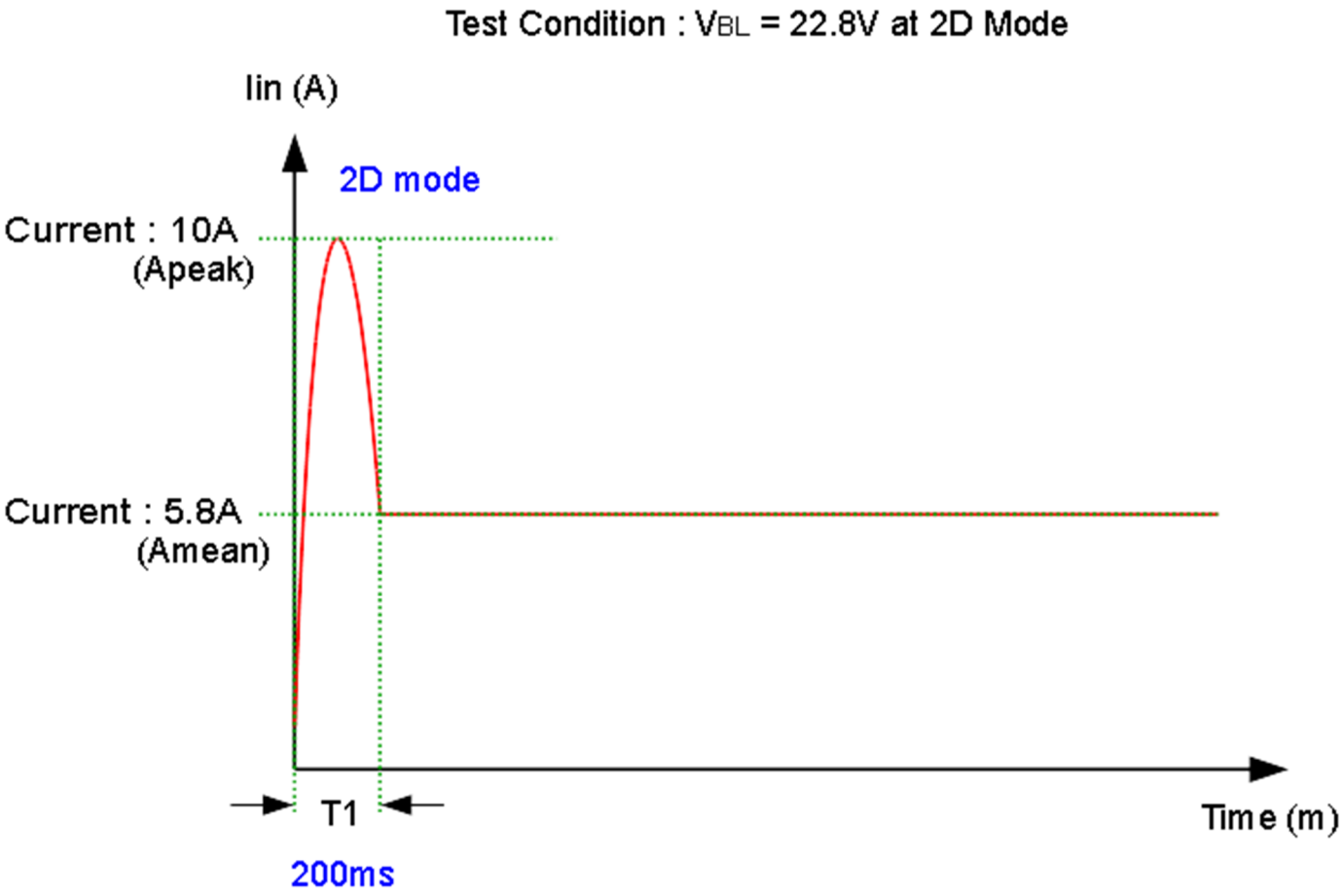
Note (2) The measurement condition of Max. value is based on 85" backlight unit under input voltage 24V, at 2D Mode and lighting 1 hour later.

Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 20ms.

Note (4) EPWM signal have to input available duty range. Between 97% and 100% duty (DDR) have to be avoided. (97% < DDR < 100%) But 100% duty (DDR) is possible. 5% duty (DDR) is only valid for electrical operation.

Note (5) FB and DDR are available only at 2D Mode.

Note (6) Below diagram is only for power supply design reference.



Note (7) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value,
Operating condition: Continuous operating at Ta = 25±2℃

3.2.2 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.25	V	Duty on	(5), (6)
	LO		—	0	—	0.8	V	Duty off	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open	
VBL Rising Time		Tr1	—	20	—	—	ms	10%-90%V_{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us	(6)	
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		TPWM	—	100	—	—	ms	(6)	
BLON Delay Time		T_{on}	—	300	—	—	ms		
		T_{on1}	—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status. Please refers to Fig.2.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

Note (6) EPWM is available only at 2D Mode.

Note (7) EPWM signal have to input available frequency range.

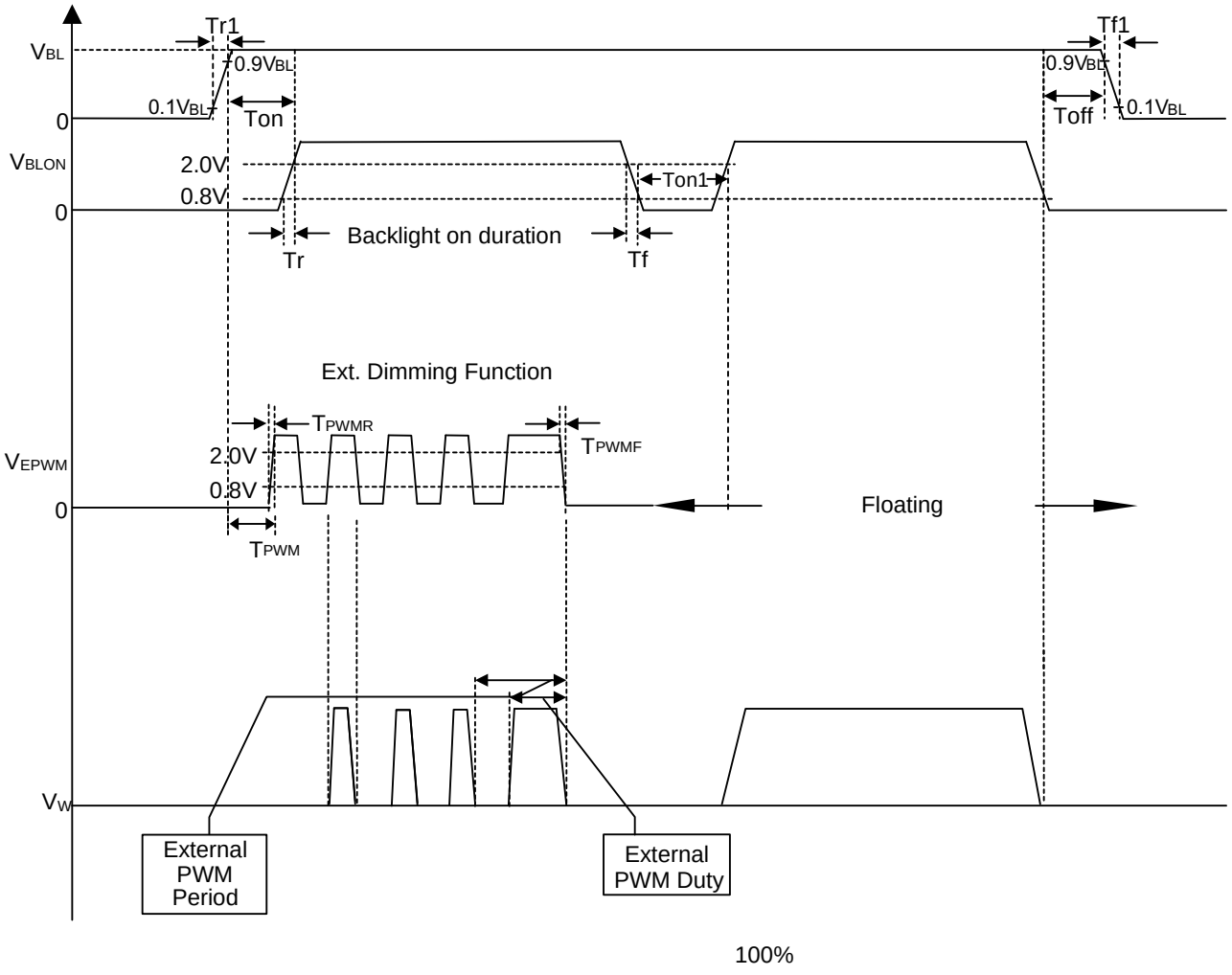


Fig. 1

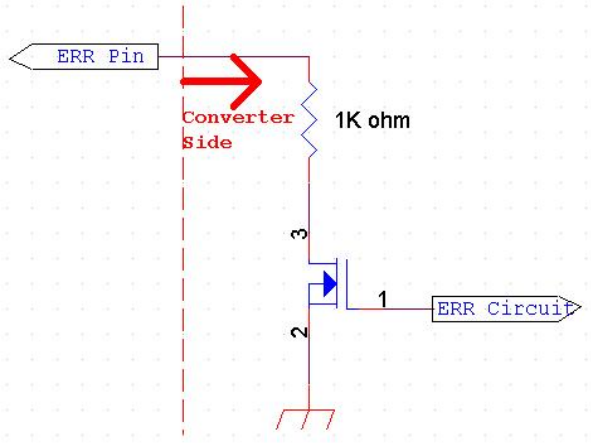


Fig. 2

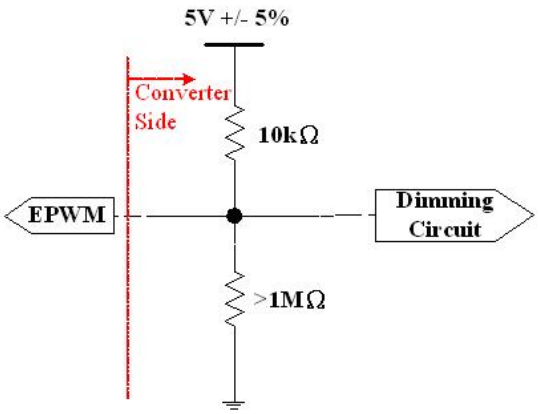


Fig. 3

4. INPUT TERMINAL PIN ASSIGNMENT

4.1 TFT LCD MODULE

CNC08 Connector Pin Assignment: [5-05162216-1(XDYT), FF01-42T-5131(FCN)]

Matting Connector

Pin	Name	Description	Note
1	N.C.	No Connection	(4)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	N.C.	No Connection	(4)
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	
15	N.C.	No Connection	(4)
16	N.C.	No Connection	(4)
17	N.C.	No Connection	(4)
18	N.C	No Connection	(4)
19	N.C	No Connection	(4)
20	N.C.	No Connection	(4)
21	N.C.	No Connection	(4)
22	LD_EN	Local Dimming Mode Enable.	
23	N.C.	No Connection	(4)
24	N.C.	No Connection	(4)
25	HTPDN	No Connection or ground	(6)
26	LOCKN	Lock detect output, Open drain.	
27	GND	Ground	
28	RX0N	1ST Pixel Negative VbyOne differential data input in area A. Lan 0	(1)

29	RX0P	1ST Pixel Positive VbyOne differential data input in area A. Lan 0	(1)
30	GND	Ground	
31	RX1N	2ND Pixel Negative VbyOne differential data input in area A. Lan 1	(1)
32	RX1P	2ND Pixel Positive VbyOne differential data input in area A. Lan 1	
33	GND	Ground	
34	RX2N	3RD Pixel Negative VbyOne differential data input in area A. Lan 2	(1)
35	RX2P	3RD Pixel Positive VbyOne differential data input in area A. Lan 2	
36	GND	Ground	
37	RX3N	4TH Pixel Negative VbyOne differential data input in area A. Lan 3	(1)
38	RX3P	4TH Pixel Positive VbyOne differential data input in area A. Lan 3	
39	GND	Ground	
40	RX4N	5TH Pixel Negative VbyOne differential data input in area A. Lan 4	(1)
41	RX4P	5TH Pixel Positive VbyOne differential data input in area A. Lan 4	
42	GND	Ground	
43	RX5N	6TH Pixel Negative VbyOne differential data input in area A. Lan 5	(1)
44	RX5P	6TH Pixel Positive VbyOne differential data input in area A. Lan 5	
45	GND	Ground	
46	RX6N	7TH Pixel Negative VbyOne differential data input in area A. Lan 6	(1)
47	RX6P	7TH Pixel Positive VbyOne differential data input in area A. Lan 6	
48	GND	Ground	
49	RX7N	8TH Pixel Negative VbyOne differential data input in area A. Lan 7	(1)
50	RX7P	8TH Pixel Positive VbyOne differential data input in area A. Lan 7	
51	GND	Ground	

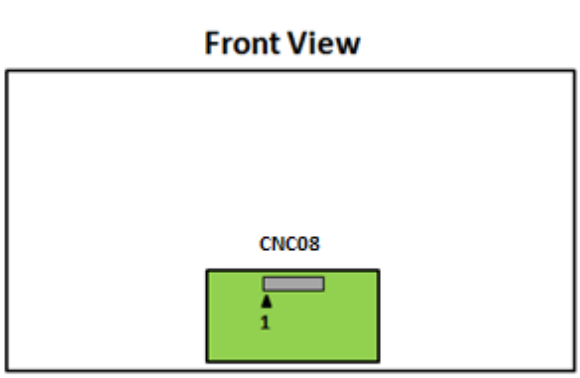
CNC07 Connector Pin Assignment: [CI0105M1HR0-LA-NH(瀚荃), JH2-D4-053N(全康-FCN)]

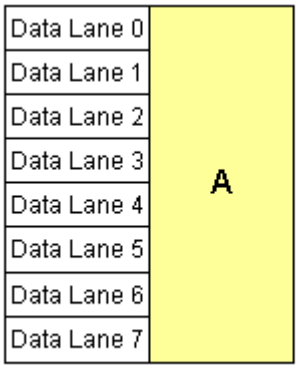
Matting connector: [PHR5(JST)]

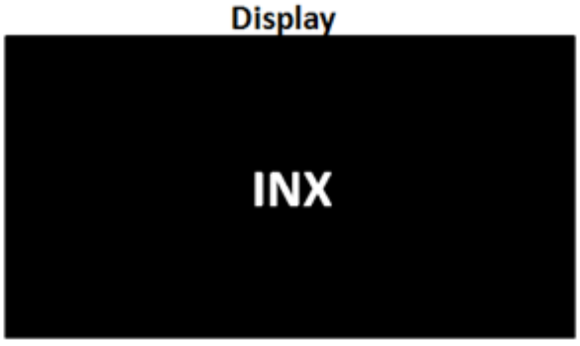
1	GND	Ground	
2	GND	Ground	
3	Vin	Power input (+12V)	(5)
4	Vin	Power input (+12V)	
5	Vin	Power input (+12V)	

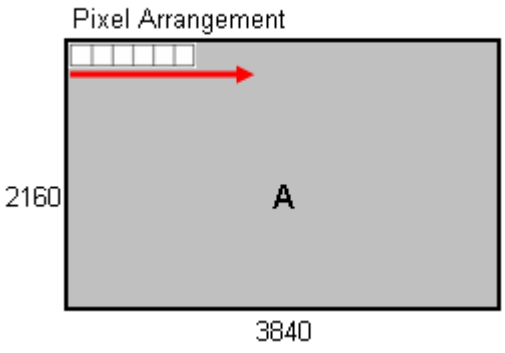
Note (1) V-by-One HS Data Mapping

Area	Lane	Data Stream
A	Lane 0	1, 9, 17, ..., 3825, 3833
	Lane 1	2, 10, 18, ..., 3826, 3834
	Lane 2	3, 11, 19, ..., 3827, 3835
	Lane 3	4, 12, 20, ..., 3828, 3836
	Lane 4	5, 13, 21, ...,3829, 3837
	Lane 5	6, 14, 22, ..., 3830, 3838
	Lane 6	7, 15, 23, ..., 3831, 3839
	Lane7	8, 16, 24, ..., 3832, 3840

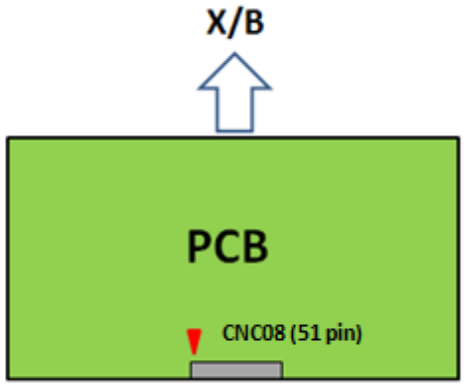




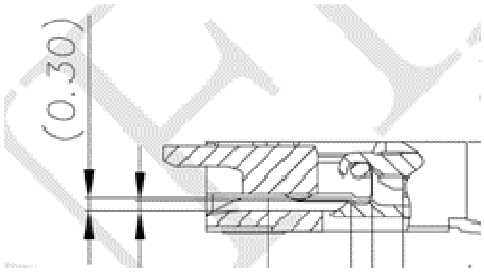




Note (2) V-by-One HS connector pin order defined as follows



Note (3) V-by-One connector mating dimension range request is 0.27mm~0.33mm as below

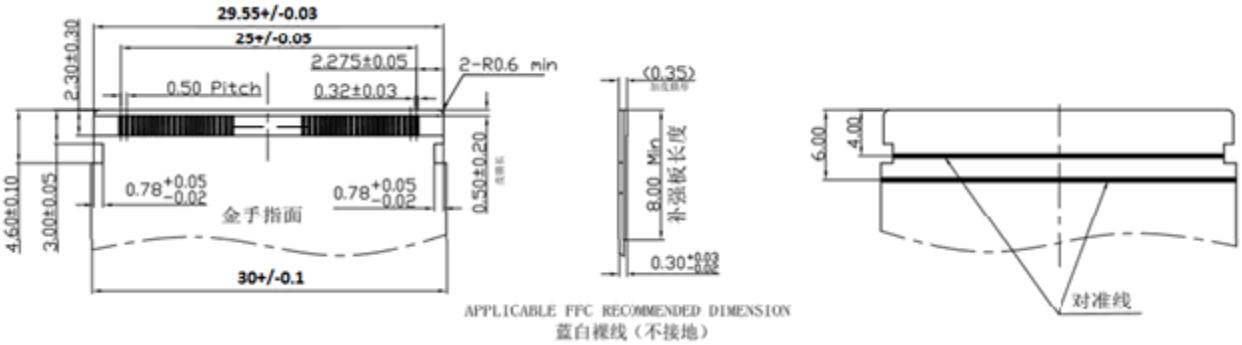


Note (4) Reserved for internal use. Please leave it open.

Note (5) Power input (+12V), Please check the current rating of FFC cable to meet the power consumption requirement.

Note (6) This pin connect to ground internal, but it could be open

Note (7) V-by-One connector Recommend Mating FFC drawing as below.



4.2 BACKLIGHT UNIT

4.2.1 LIGHT BAR UNIT

The pin configuration for the housing and lead wire is shown in the table below.

CNL01 Connector Pin Assignment: [TBD]

Pin №	Symbol	Feature
1	VLED2+	Positive of LED String
2	VLED2+	Positive of LED String
3	VLED2+	Positive of LED String
4	VLED-	Negative of LED String
5	VLED-	Negative of LED String
6	VLED-	Negative of LED String
7	VLED-	Negative of LED String
8	VLED-	Negative of LED String
9	VLED-	Negative of LED String
10	VLED-	Negative of LED String
11	VLED-	Negative of LED String
12	VLED-	Negative of LED String
13	VLED-	Negative of LED String
14	VLED-	Negative of LED String
15	VLED-	Negative of LED String
16	VLED1+	Positive of LED String
17	VLED1+	Positive of LED String
18	VLED1+	Positive of LED String

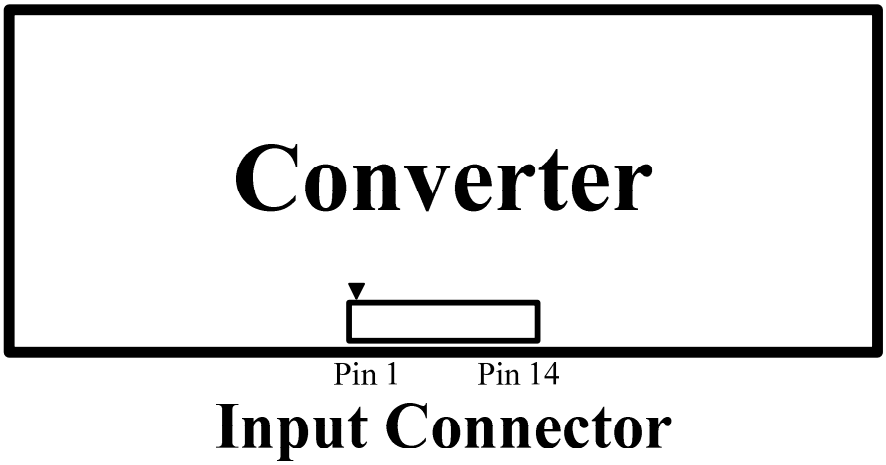
Note (1) Light Bar Input connector pin order defined as follows

4.2.2 CONVERTER UNIT

CNV1 Connector Pin Assignment: [CI0114M1HR0-LA (CvilLux) , JH2-D4-143N (FCN)]
Matting connector : [JST PHR-14]

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) ; Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

Note (1) Input connector pin order defined as follows

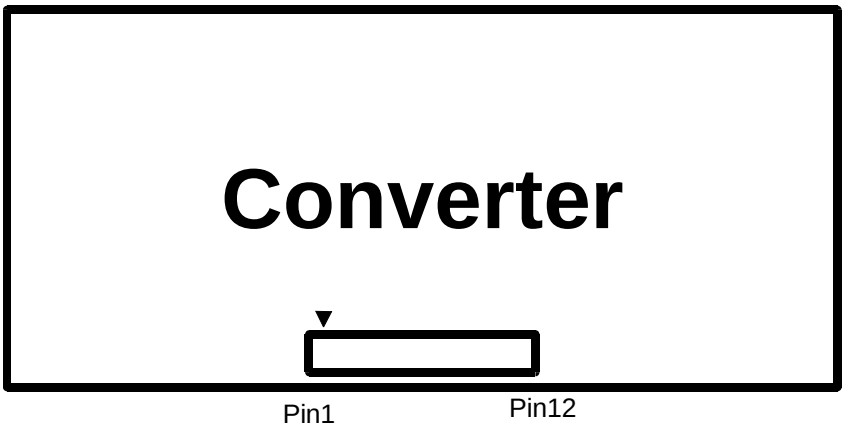


Input Connector

CNV02 Connector Pin Assignment: [CI0112M1HR0-LA (CvilLux) or JH2-D4-123N (FCN)]
Matting connector : [JST PHR-12]

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

Note (1) Input connector pin order defined as follows



Input Connector

5. INTERFACE TIMING

5.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. (Ta = 25 ± 2 ºC)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frequency	Data Clock	1/Tc	70	74.25	80	MHz	(1)
VbyOne Receiver	Intra-Pair skew		-0.3		0.3	UI	(2)
	Inter-Pair skew		- 5		5	UI	(3)
	Spread spectrum modulation range	F_{clkin_mod}	1/Tc-0.5%	—	1/Tc+0.5%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	30	KHz	

5.1.1 INPUT TIMING SPEC FOR UHD, FRAME RATE = 50HZ

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		Fr5	47	50	53	Hz	(5),(6)
Horizontal Frequency			Fh	122.8	135	140	KHz	
Vertical Active Display Term (8 Lan,3840X2160 Active Area)	2D Mode	Total	Tv	2200	2700	2790	Th	Tv=Tvd+Tvb
		Display	Tvd	2160	2160	2160	Th	
		Blank	Tvb	40	540	630	Th	
Horizontal Active Display Term (8 Lan,3840X2160 Active Area)	2D Mode	Total	Th	530	550	570	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	
		Blank	Thb	50	70	90	Tc	

5.1.2 INPUT TIMING SPEC FOR UHD, FRAME RATE = 60HZ

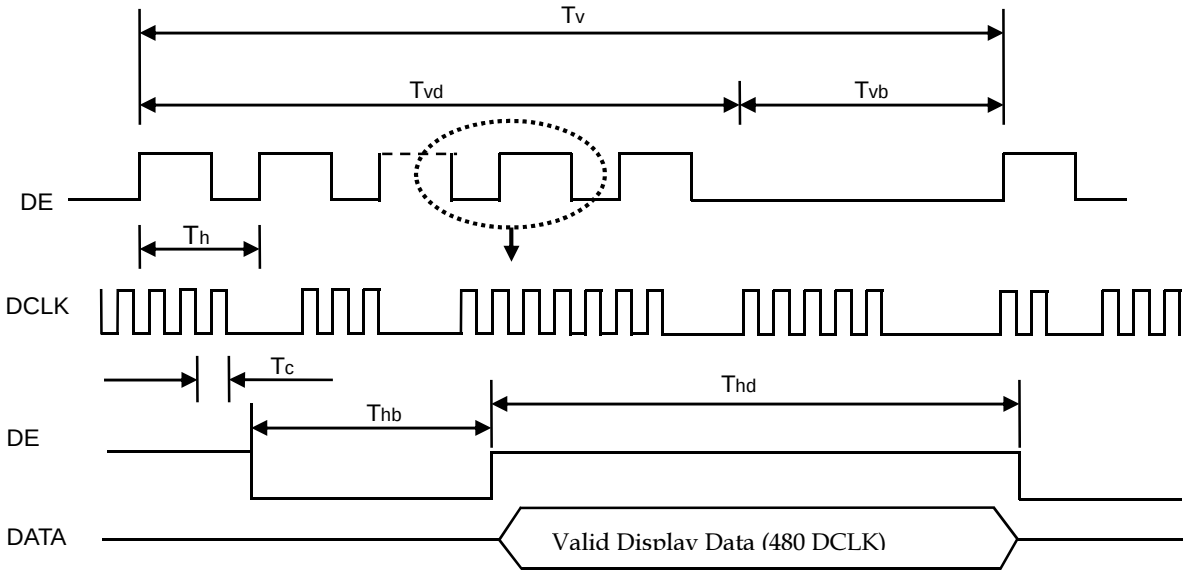
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		Fr6	57	60	63	Hz	(5),(6)
Horizontal Frequency			Fh	122.8	135	140	KHz	
Vertical Active Display Term (8 Lan, 3840X2160 Active Area)	2D Mode	Total	Tv	2200	2250	2790	Th	Tv=Tvd+Tvb
		Display	Tvd	2160	2160	2160	Th	—
		Blank	Tvb	40	90	630	Th	—
Horizontal Active Display Term (8 Lan, 3840X2160 Active Area)	2D Mode	Total	Th	530	550	570	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	50	70	90	Tc	—

Note (1) Please make sure the range of pixel clock has follow the below equation：

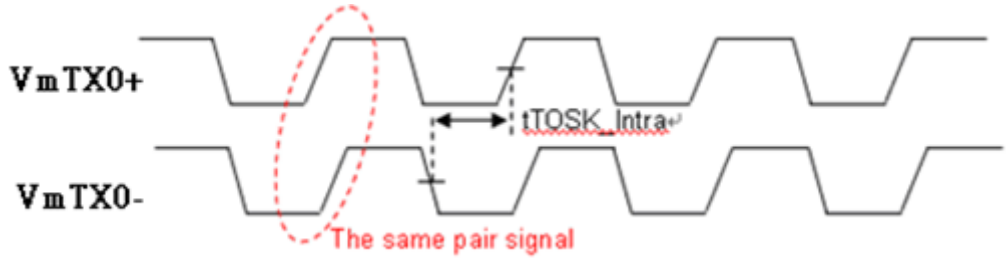
Fclkin(max) ≧ Fr × Tv × Th

Fr × Tv × Th ≧ Fclkin (min)

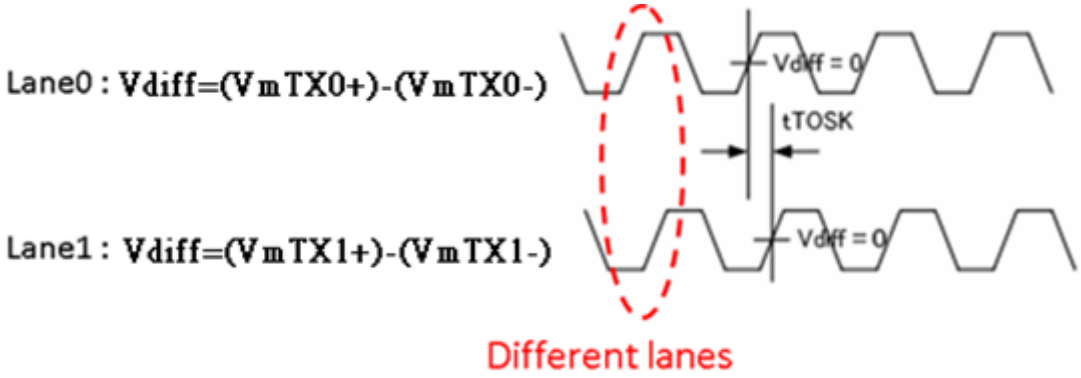
INPUT SIGNAL TIMING DIAGRAM



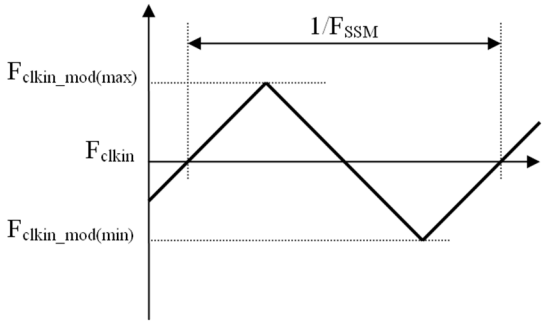
Note (2) VbyOne HS Intra-pair skew



Note (3) VbyOne HS Inter-pair skew

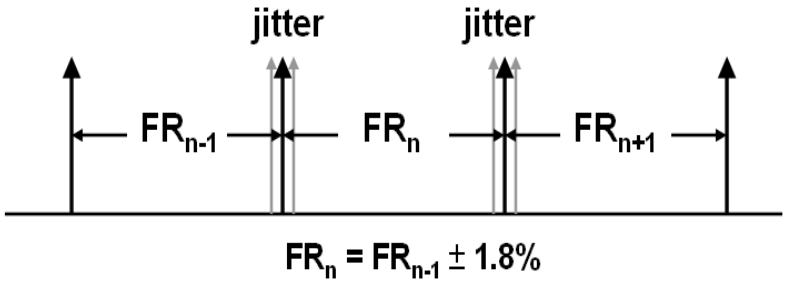


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) For converter reference signals, The frame-to-frame jitter of the input frame rate is defined as the above figures. FRn = FRn-1 ± 1.8%.

Note (6) For converter reference signals, The setup of the frame rate jitter > 1.8% may result in the cosmetic LED backlight symptom.



5.2 TIMING DIAGRAM

5.2.1 V BY ONE SIGNAL TIMING DIAGRAM

The eye diagram is measured by the oscilloscope and receiver CDR characteristic must be emulated.

PLL bandwidth: 40MHz

Damping facto: 1.4

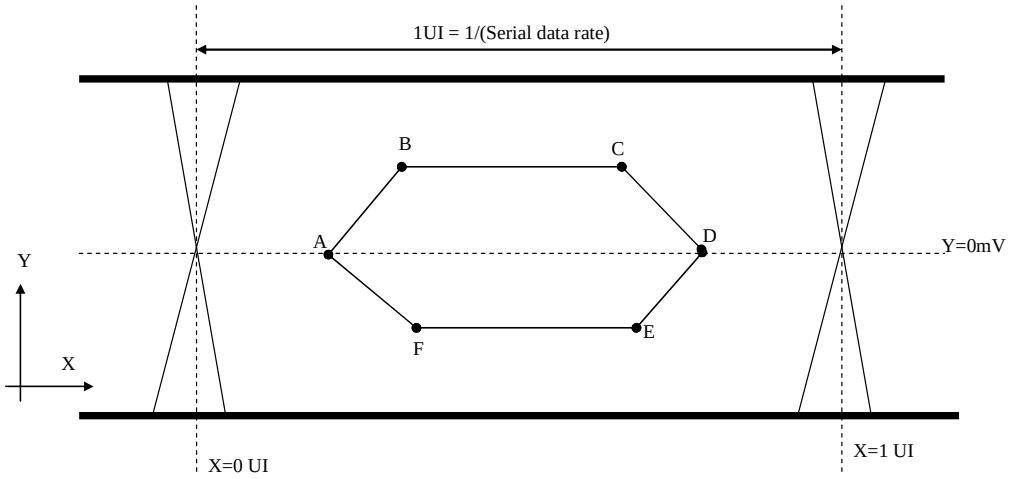


Table 1 Eye Mask Specification

	X [UI]	Y [mV]	Note
A	0.25	0	(1)
B	0.3	50	(1)
C	0.7	50	(1)
D	0.75	0	(1)
E	0.7	-50	(1)
F	0.3	-50	(1)

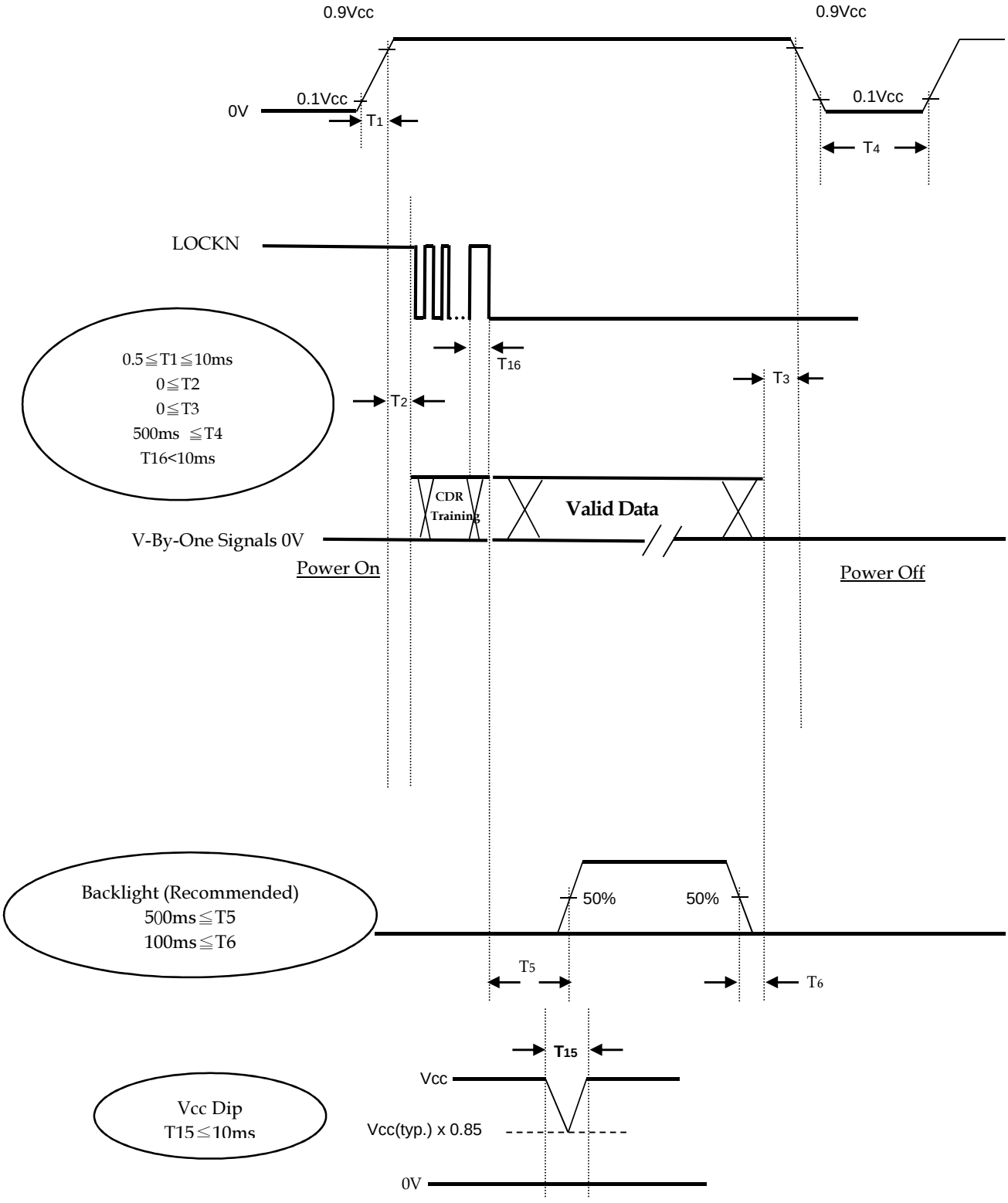
Note (1) Input levels of V-by-One HS signals are comes from "V-by-One HS Stander Ver.1.4"

5.3 BYTE LENGTH AND COLOR MAPPING OF V-BY-ONE HS

Packer input & Unpacker output		30bpp RGB (10bit)
Byte 0	D[0]	R[2]
	D[1]	R[3]
	D[2]	R[4]
	D[3]	R[5]
	D[4]	R[6]
	D[5]	R[7]
	D[6]	R[8]
	D[7]	R[9]
Byte 1	D[8]	G[2]
	D[9]	G[3]
	D[10]	G[4]
	D[11]	G[5]
	D[12]	G[6]
	D[13]	G[7]
	D[14]	G[8]
	D[15]	G[9]
Byte 2	D[16]	B[2]
	D[17]	B[3]
	D[18]	B[4]
	D[19]	B[5]
	D[20]	B[6]
	D[21]	B[7]
	D[22]	B[8]
	D[23]	B[9]
Byte 3	D[24]	X
	D[25]	X
	D[26]	B[0]
	D[27]	B[1]
	D[28]	G[0]
	D[29]	G[1]
	D[30]	R[0]
	D[31]	R[1]

5.4 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance besides HTPDN and LOCKN. If T2<0, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) Vcc must decay smoothly when power-off.

Note (7) HTPDN(internal ground) : For customer reference signal. It can be ignored if customer not use.

Note (8) T16 , V-by-One signals shall be stabilized and follows timing specification which defined by section 5.1&5.2

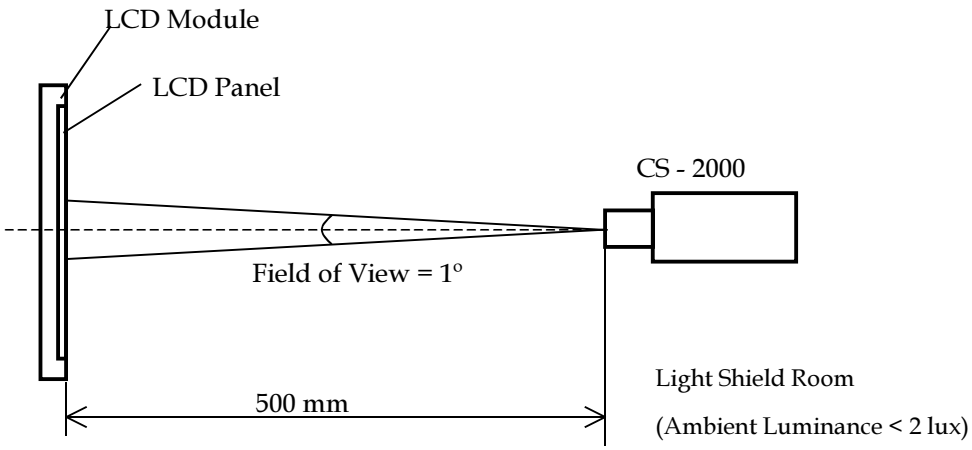
6. OPTICAL CHARACTERISTICS

6.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.

Local Dimming Function should be Disable before testing to get the steady optical characteristics (According to 5.1 CNF1 Connector Pin Assignment, Pin no. "22")



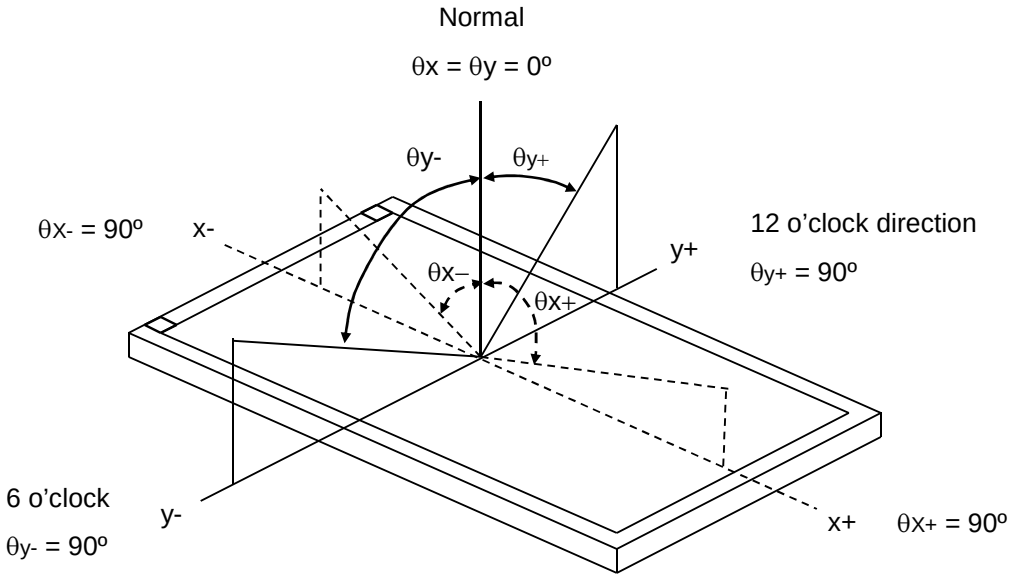
6.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 6.2. The following items should be measured under the test conditions described in 6.1 and stable environment shown in 6.1.

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		θ_x=0°, θ_Y =0° Viewing angle at normal direction	3500	5000		-	Note (2)
Response Time		Gray to gray				11	22	ms	Note (3)
Center Luminance of White		L_C	2D		2000	2500		cd/m²	Note (4)
White Variation		δW					1.3	-	Note (6)
Cross Talk		CT	2D				4	%	Note (5)
Color Chromaticity	Red	Rx			Typ.-0.03	(0.644)	Typ.+0.03	-	
		Ry				(0.337)		-	
	Green	Gx				(0.308)		-	
		Gy				(0.617)		-	
	Blue	Bx				(0.152)		-	
		By				(0.052)		-	
	White	Wx				0.280		-	
		Wy				0.290		-	
	Correlated color temperature				-	10000	-	K	
	Color Gamut	C.G.			-	72	-	%	NTSC
Viewing Angle	Horizontal	θ_x+		CR≥10	80	89	-	Deg.	(1)
		θ_x-			80	89	-		
	Vertical	θ_Y+			80	89	-		
		θ_Y-			80	89	-		

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R).



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

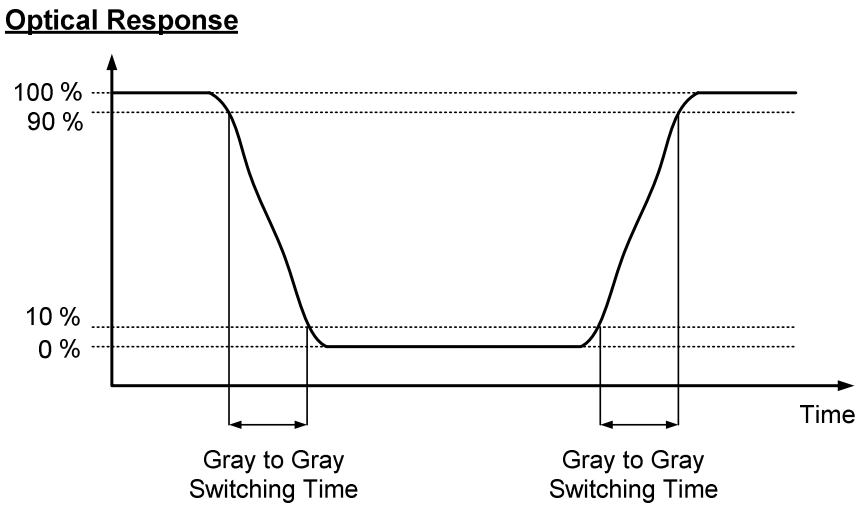
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time :



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (4) Definition of Luminance of White (L_C) :

Measure the luminance of gray level 1023 at center point.

L_C = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (6).

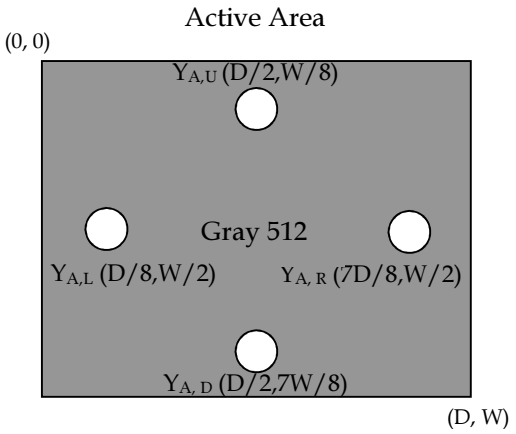
Note (5) Definition of Cross Talk (CT) :

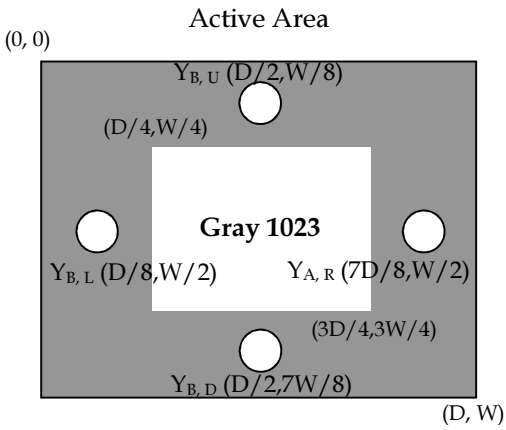
$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where :

YA = Luminance of measured location without gray level 1023 pattern (cd/m2)

YB = Luminance of measured location with gray level 1023 pattern (cd/m2)

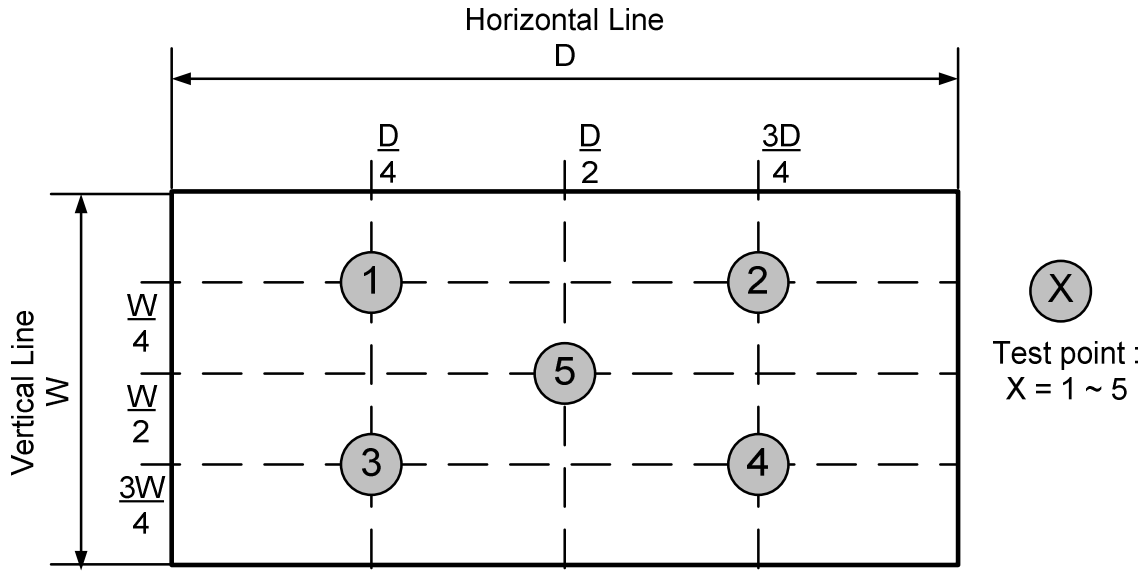




Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

$$\delta W = \frac{\text{Maximum}[L(1), L(2), L(3), L(4), L(5)]}{\text{Minimum}[L(1), L(2), L(3), L(4), L(5)]}$$



Note (7) Strong light exposure causes degradation of polarizer and color filter.

7. PRECAUTIONS

7.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[3] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.

[4] It should be attached to the system firmly using all mounting holes.

[5] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer, do not press or scratch the surface harder than a HB pencil lead.

[6] Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

[7] Protection film for polarizer on the module should be slowly peeled off just before use so that the electrostatic charge can be minimized.

[8] Do not disassemble the module.

[9] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[10] Do not plug in or pull out the I/F connector while the module is in operation, pins of I/F connector should not be touched directly with bare hands. Do not adjust the variable resistor located on the module.

[11] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[12] When storing modules as spares for a long time, the following precaution is necessary.

[12.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity (under 70%) without condensation.

[12.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[13] Use a soft dry cloth without chemicals and Ethyl Alcohol for cleaning, because the surface of polarizer is very soft and easily scratched. Do not use Ketone type materials (ex. Acetone), Toluene, Ethyl acid or Methyl chloride, these chemical solvent might permanently damage the polarizer due to chemical action.

7.2 SAFETY PRECAUTIONS

To optimize PID module's lifetime and functions, operating conditions should be followed as below

[1] Normal operating condition

[1.1] Well-ventilated place is suggested to set up PID module and system.

[1.2] Display pattern : regular switched patterns or moving pictures.

[2] Operating usage to protect against image sticking due to long-term static display.

[2.1]Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.

[2.2] Periodical display contents should be changed from static image to moving picture.

[2.2.1] Different background and image colors changed respectively, and changed colors periodically.

[2.2.2] Background and image with large different luminance displayed at the same time should be avoided.

[2.2.3]Periodical power-off the system for a while or screen saver is needed after long-term static display.

[2.2.4] Moving picture or black pattern is strongly recommended for screen saver.

[3] The startup voltage of a Backlight may cause an electrical shock while assembling with the converter. Do not disassemble the module or insert anything into the Backlight unit.

[4] Do not connect or disconnect the module in the "Power On" condition.

[5] Do not exceed the absolute maximum rating value. (supply voltage variation, input voltage variation, variation in part contents and environmental temperature…) Otherwise the module may be damaged.

[6] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[7] Module should be turned clockwise (regular front view perspective) when used in portrait mode.

[8] Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, especially combining severe conditions such as high temperature/humidity, display stationary patterns, or long operation time etc…, it is strongly recommended to contact INX for field application engineering advice. Otherwise, the panel may be damaged and its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and full outdoor display.

[9] LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.

7.3 PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter. Since the product design is not protected by ultra-violet ray filter, the deterioration of the polarizer due to sun exposure or water drenching is not guarantee.

7.4 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

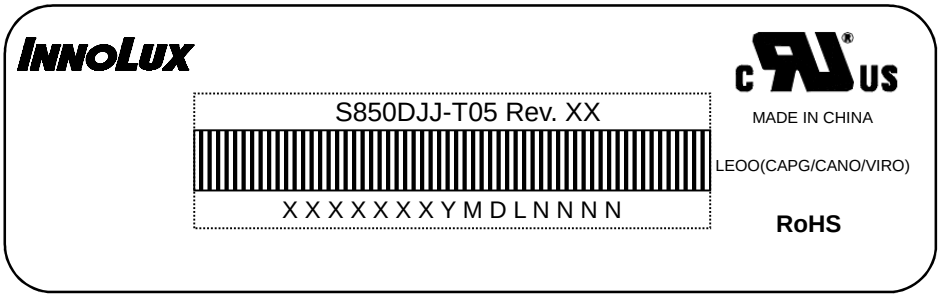
Regulatory	Item	Standard
Audio/video, Information and Communication Technology Equipment	UL	UL 62368-1, 3rd Ed, 2021-10-22
	cUL	CAN/CSA C22.2 No. 62368-1:19, 3rd Ed, 2021-10-22
	CB	IEC 62368-1:2018 EN IEC 62368-1:2020+A11:2020

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

8. DEFINITION OF LABELS

8.1 MODULE LABEL

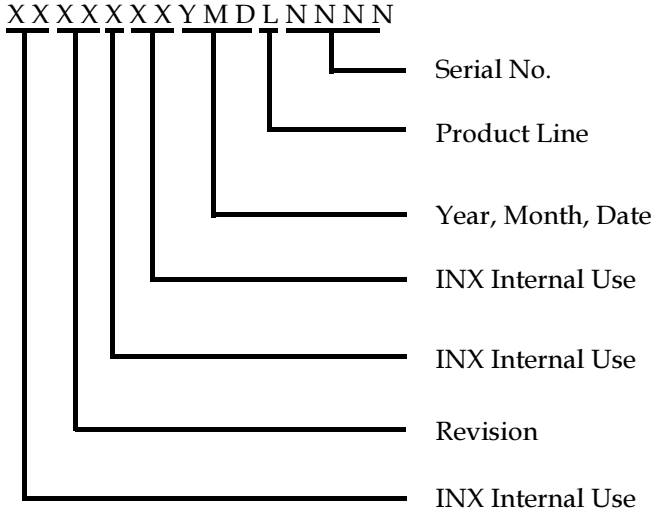
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name : S850DJJ-T05

Revision : Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID : X X X X X X Y M D L N N N N



Serial ID includes the information as below :

Manufactured Date :

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

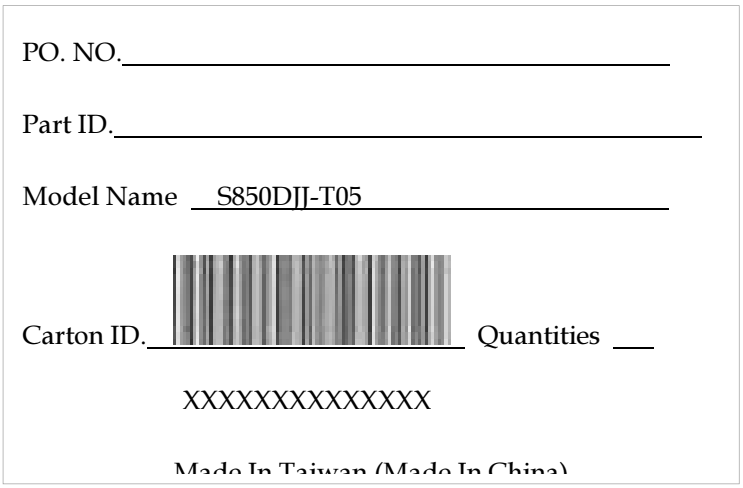
Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1→Line1, 2→Line 2, …etc.

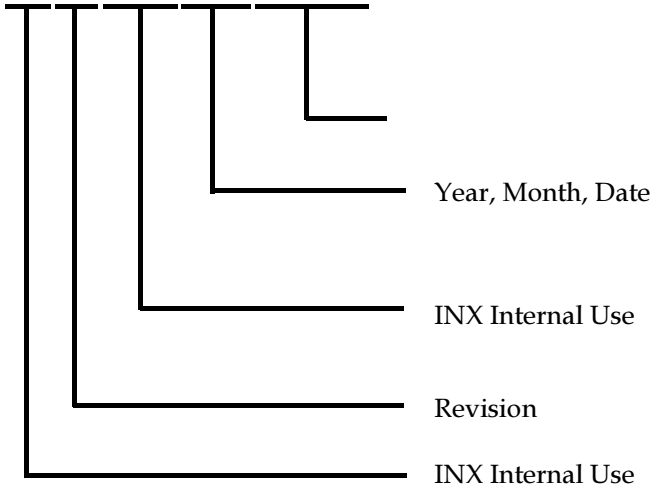
8.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.



Model Name: S850DJJ-T05

Carton ID: X X X X X X X Y M D X X X X



Serial ID includes the information as below :

Manufactured Date:

Year: 2010=0, 2011=1, 2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

9. PACKAGING

9.1 PACKAGING SPECIFICATIONS

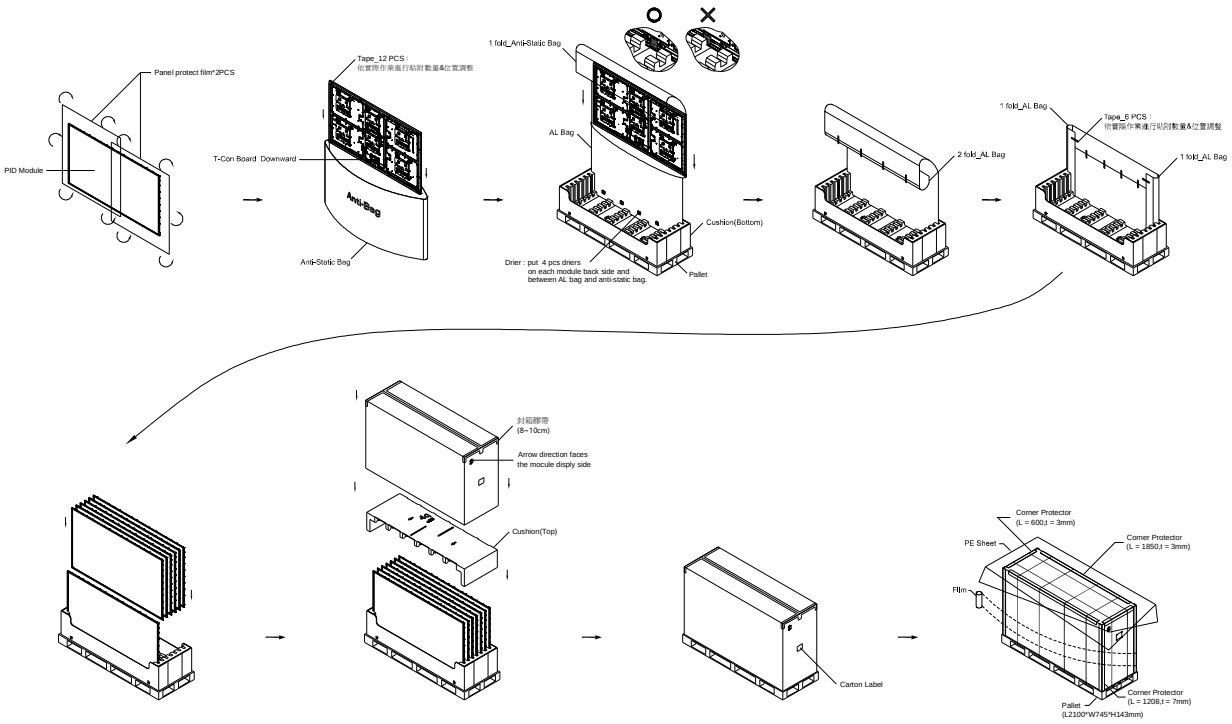
(1) 7 LCD TV modules / 1 Box

(2) Box dimensions : 2070mm(L) X 714 mm(W) X 1232mm (H)

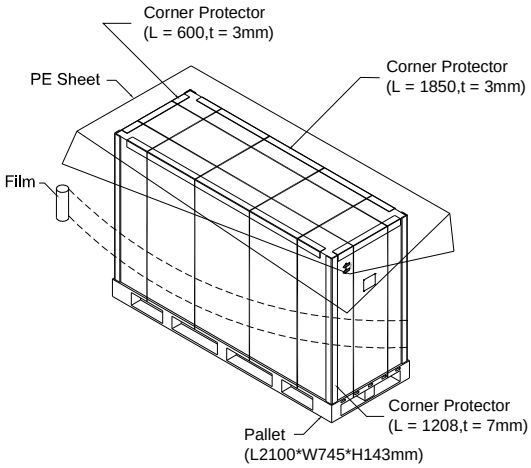
(3) Weight: approximately 398 Kg

9.2 PACKAGING METHOD

Packaging method is shown in following Figures.

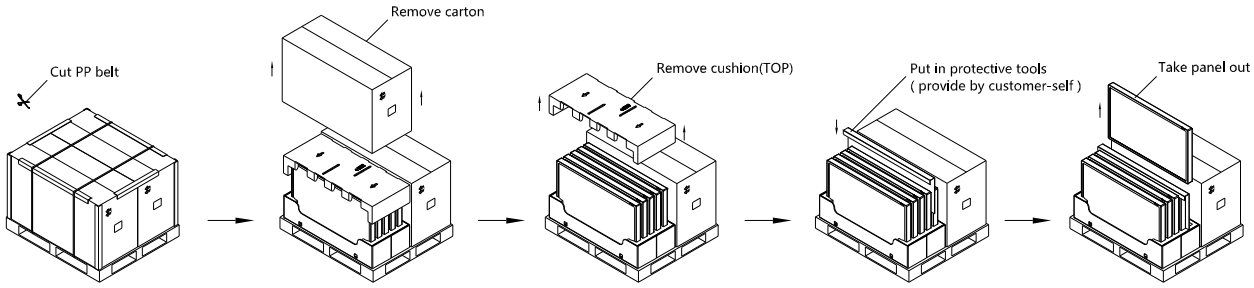


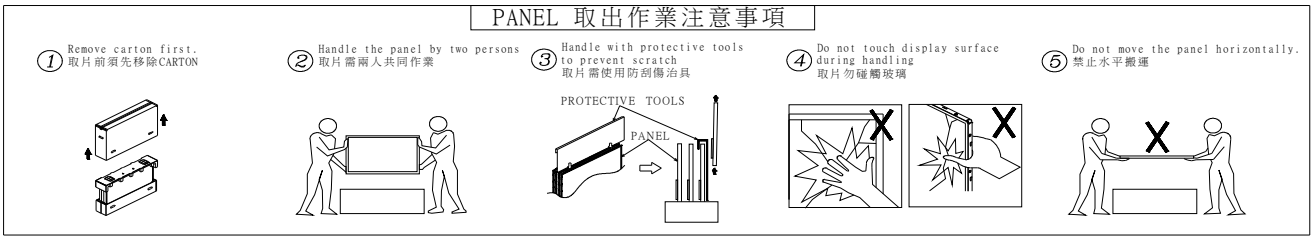
Air / Sea / Land Transportation
(40ft / 40ft HQ Container)
1 Layer



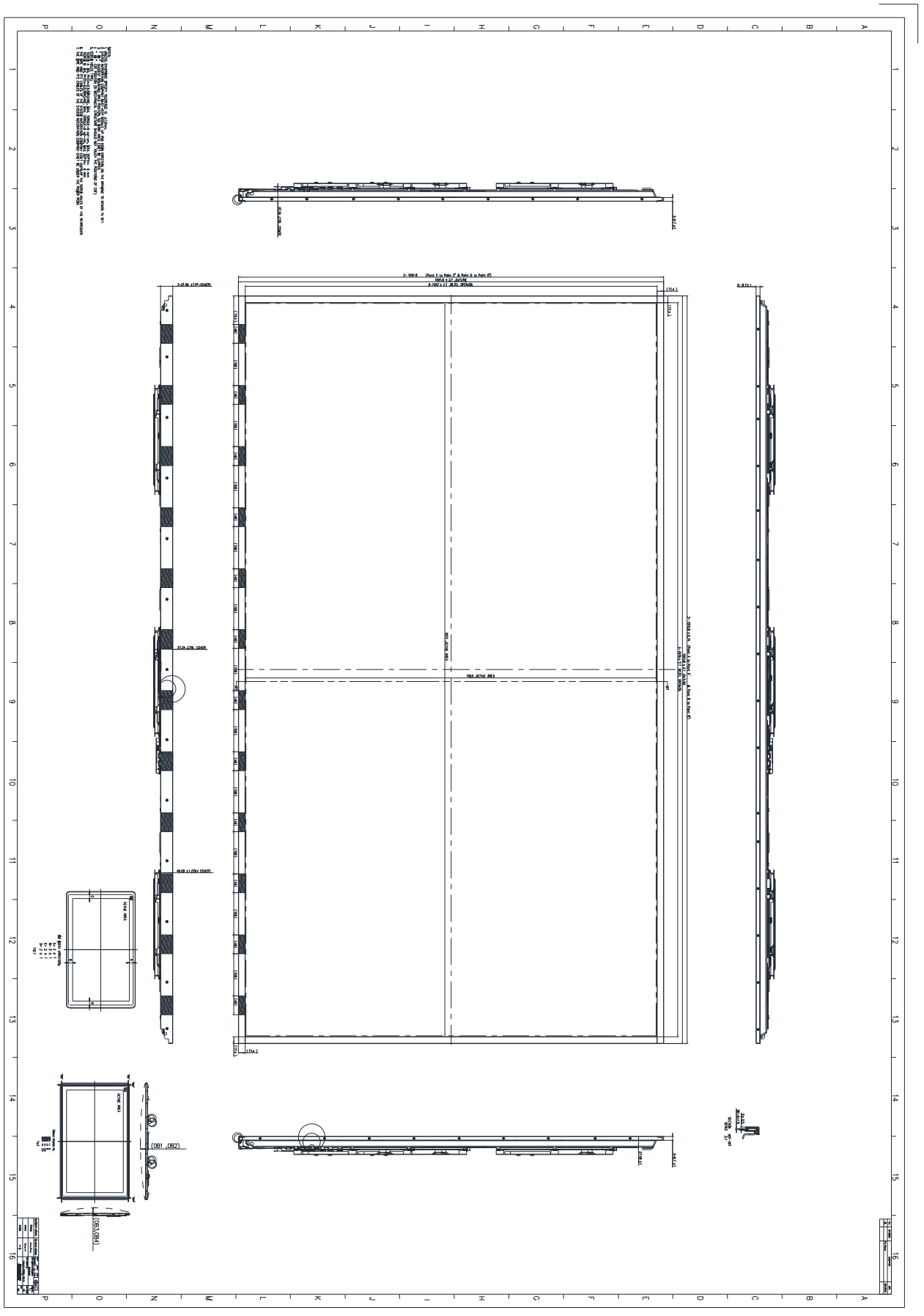
9.3 UN-PACKAGING METHOD

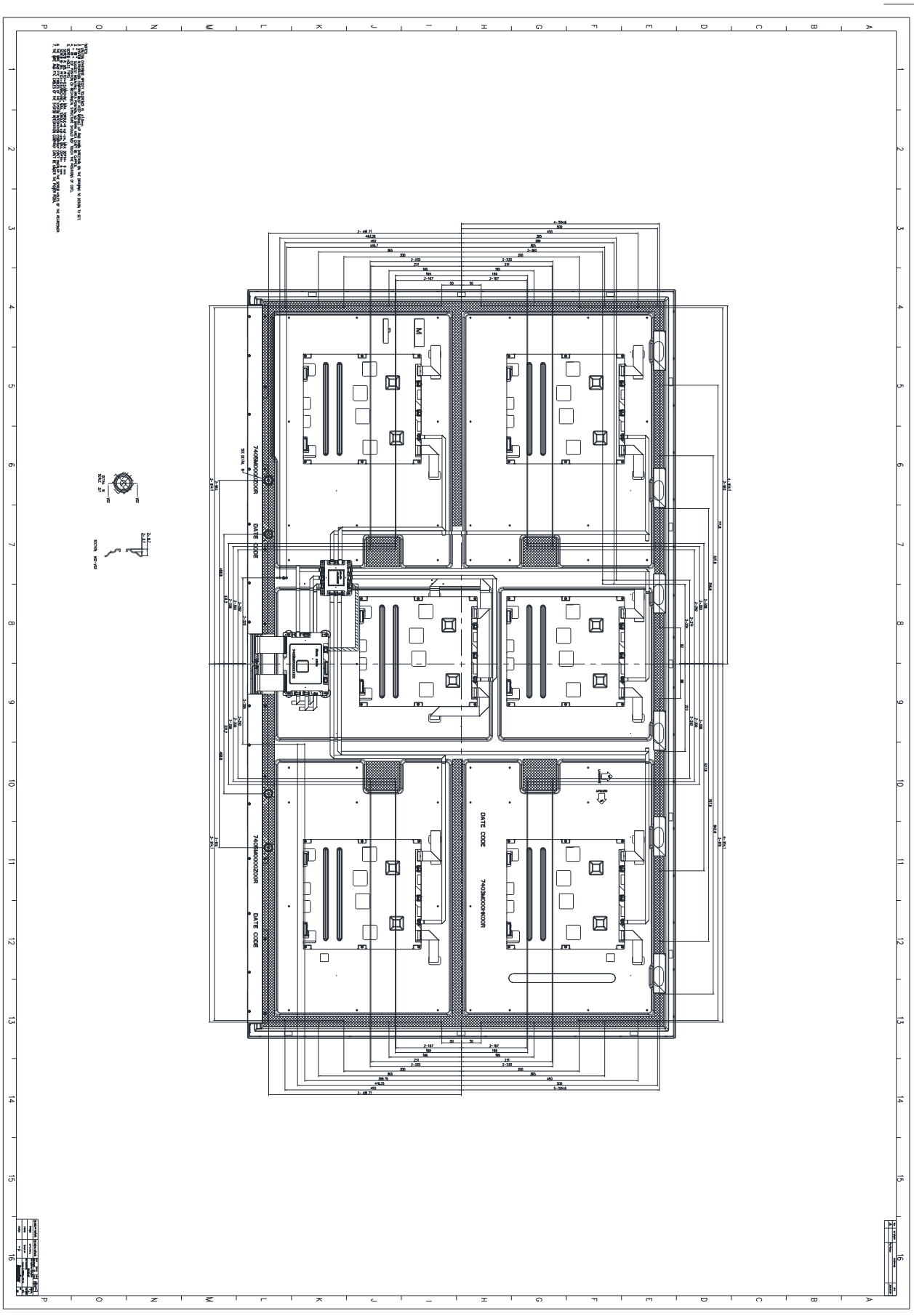
Un-packaging method is shown in following Figure.

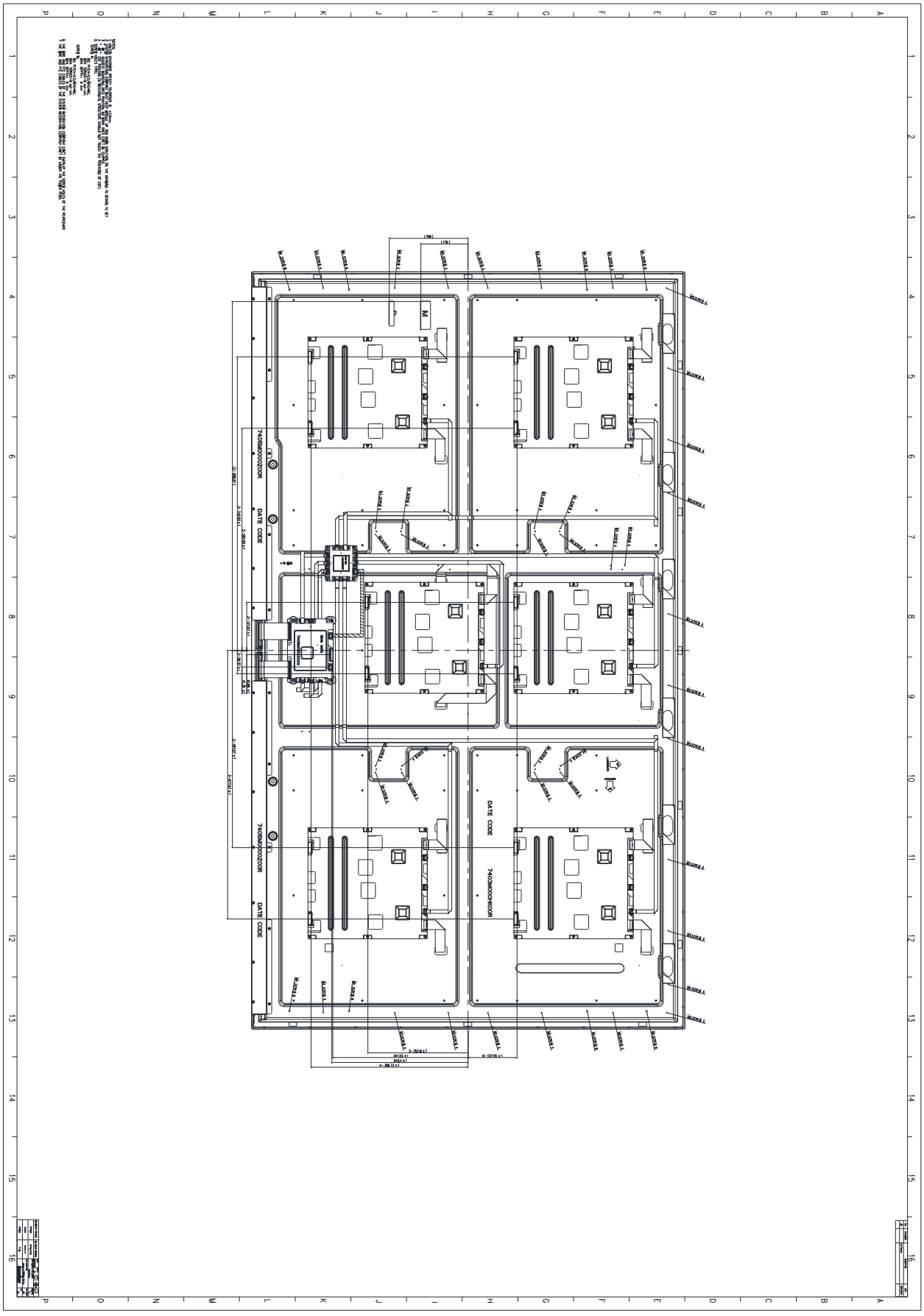


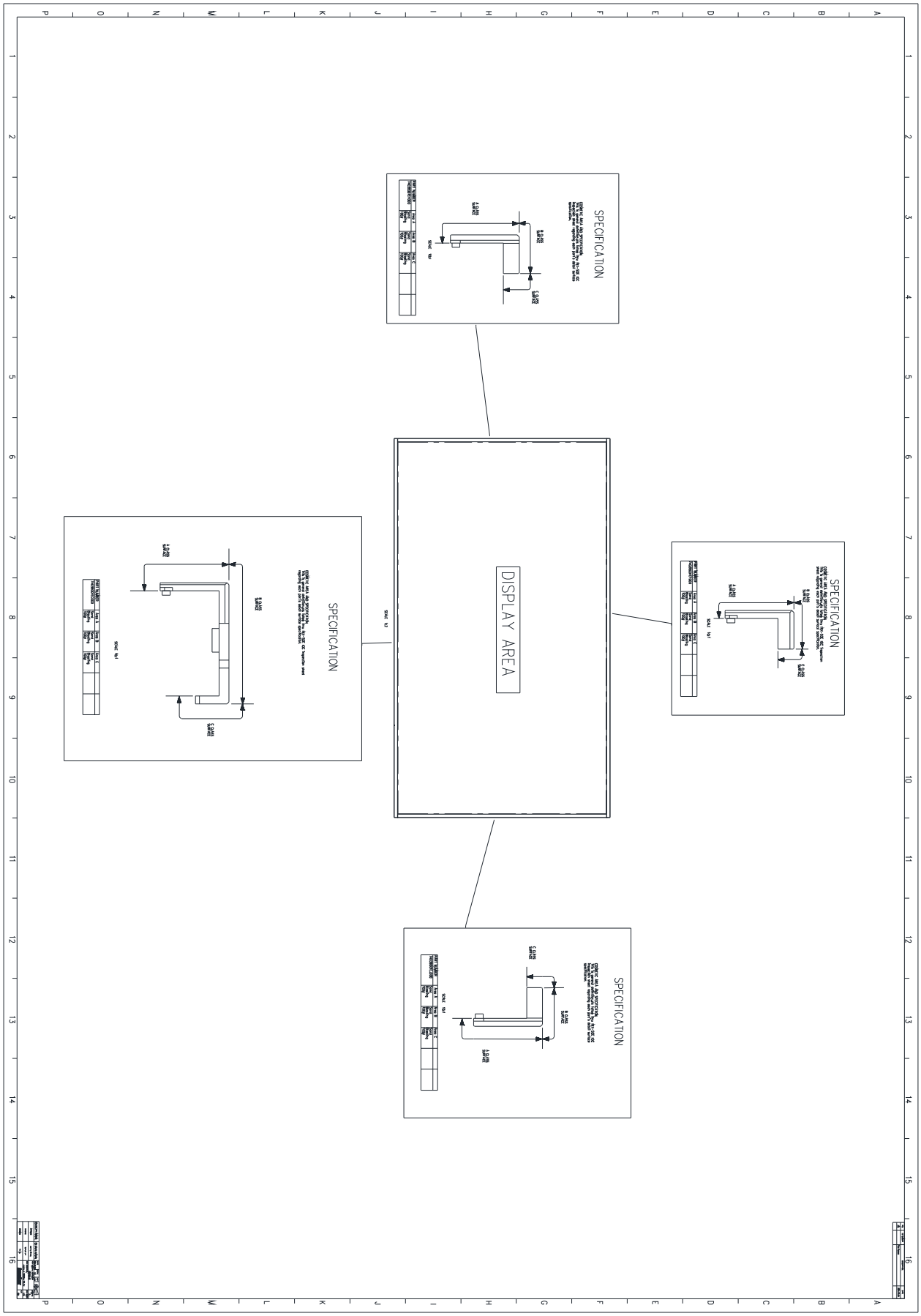


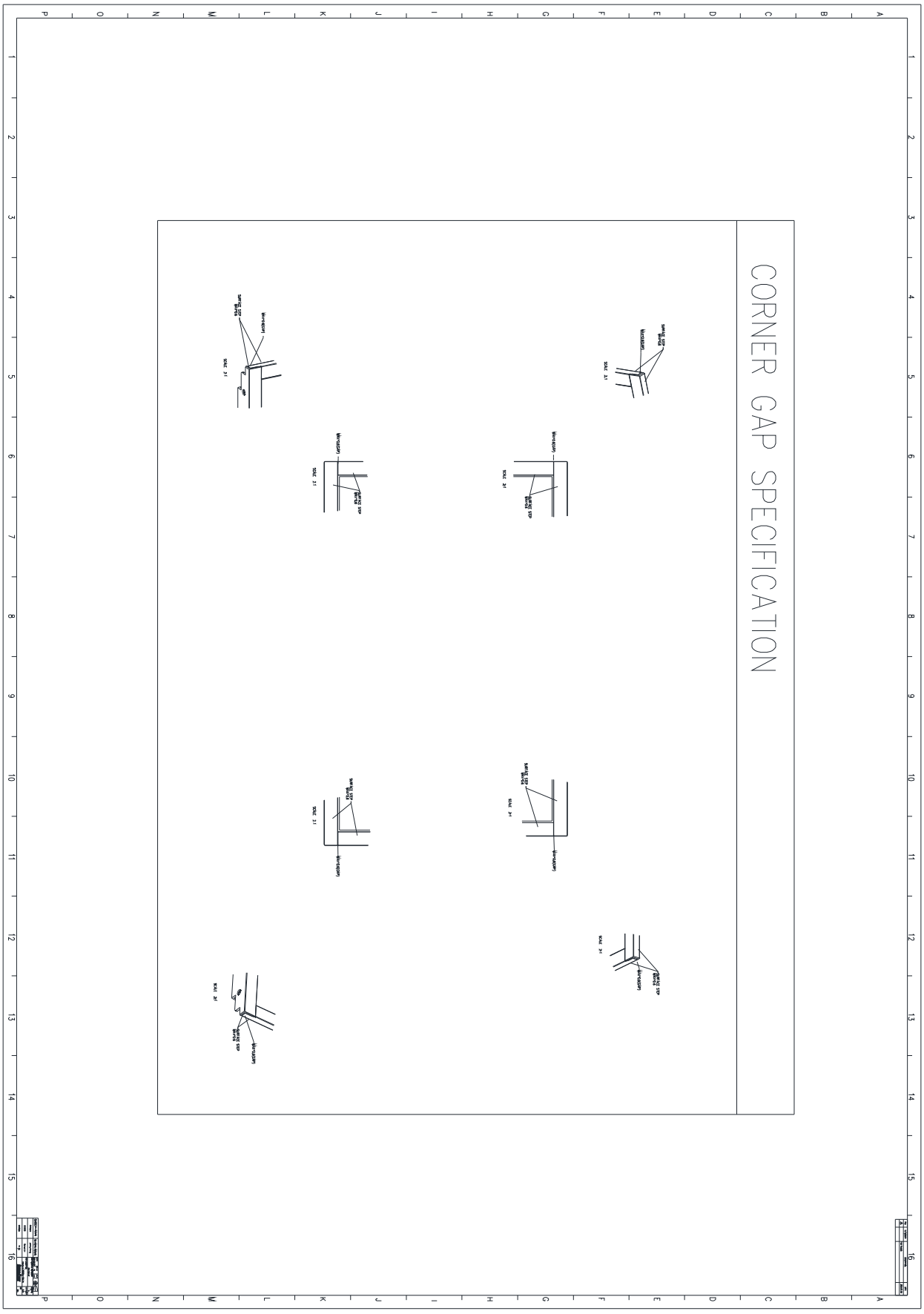
10. MECHANICAL CHARACTERISTIC











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