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Datasheet

LG Display

LP156WFD-SPM2

HD-10-156

SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**
(◆) **Final Specification**

Title	15.6” FHD TFT LCD

BUYER	General
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP156WFD
Suffix	SPM2

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

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Contents

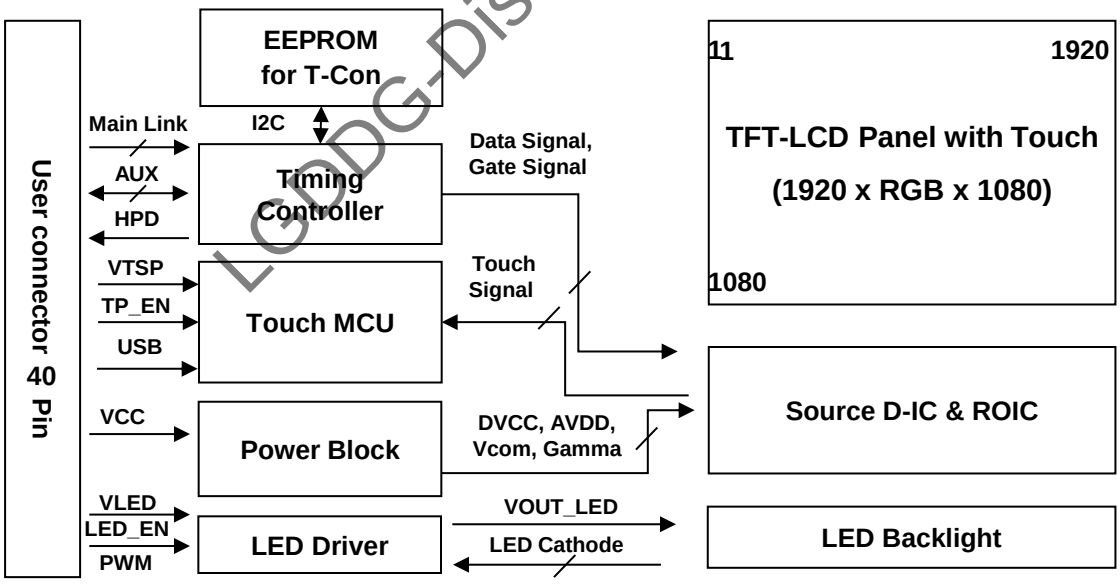
Record of Revisions

Revision No	Revision Date	Page	Before	After	EDID version
0.0	May. 27. 2019	All	First Draft (Preliminary Specification)	-	-
1.0	Jan. 51. 2020		Final CAS Release		1.0
		18	TBD	Update touch F/W version	
		19	T2: 70ms	T2: 150ms	

1. General Description

1-1. Intorduction

The LP156WFD is a Color Active Matrix Liquid Crystal Display with Advanced In-cell Touch System. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. This TFT-LCD has 15.6 inches diagonally measured active display area with FHD resolution (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors. The LP156WFD has been designed to apply the interface method that enables low power, high speed, low EMI. The LP156WFD is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP156WFD characteristics provide an excellent flat display for office automation products such as Notebook PC.



1-2. General Feature

Active Screen Size		15.6 inches diagonal
Outline Dimension		350.66mm(H, Typ.) x 216.25mm(V, Typ.) x 3.2mm(D, Max), with PCBA
Pixel Pitch		0.1793mm x 0.1793mm
Pixel Format		1920 horiz. by 1080 vert. Pixels RGB strip arrangement
Color Depth		6-bit, 262,144 colors
Luminance, White		250cd/m^2(Typ.)
Power Consumption		Total 4.19W (Max.) Logic : 0.94W (Max. @ Mosaic, w/Touch), B/L : 3.25W (Max.)
Weight		380g (Max.)
Display Operating Mode		Normally black
Surface Treatment		Anti Glare treatment (3H) of the front Polarizer
Color Gamut		NTSC 45%
LED Dimming Control mode		DC Dimming
RoHS Compliance		Yes
BFR / PVC / As Free		Yes for all
eDP version(Tcon)		eDP1.2
DPCD version		Ver1.1
Function	PSR	Not support
	sDRRS	48Hz
	DMRRS	not support
	Adaptive sync	Not support
	NVSR	not support
	SSC	down spread 5%

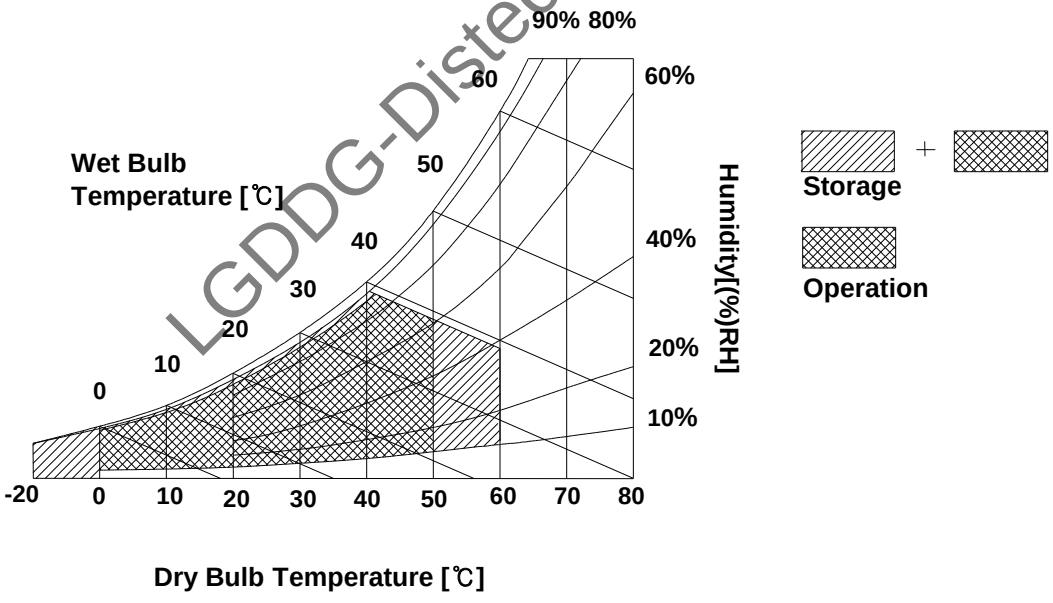
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	V_{DC}	at 25 ± 2°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	TST	-20	60	°C	1,2
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1,2

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.
Note : 2. Storage Condition is guaranteed under packing condition.



3. Electrical Specifications

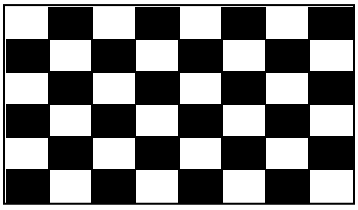
3-1. LCD Electrical Characteristics

Table 2. LCD ELECTRICAL CHARACTERISTICS

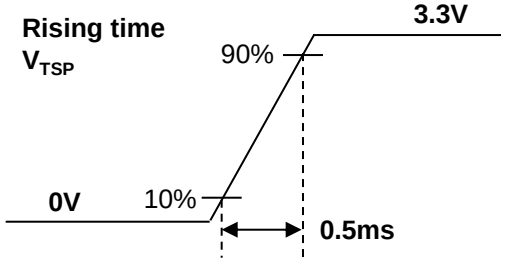
Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
VCC Power Supply Input Voltage		V_{CC}	3.0	3.3	3.6	V	1
VCC Permissive Power Supply Input Ripple		V_{CCrp}	-	-	100	mV_{p-p}	
VCC Power Supply Input Current	Mosaic /Solid	I_{CC}	-	227	255	mA	2
	Red	I_{CC}	-	360	400	mA	
VCC Power Consumption		P_{CC}	-	0.75	0.84	W	
VCC Power Supply Inrush Current		I_{CC_P}	-	-	1.5	A	3
VTSP Power Supply Input Voltage		V_{TSP}	3.0	3.3	3.6	V	1
VTSP Permissive Power Supply Input Ripple		V_{TSPrp}	-	-	100	mV_{p-p}	
VTSP Power Supply Input Current		I_{TSP}	-	27	30	mA	2
VTSP Power Consumption		P_{TSP}	-	0.09	0.10	W	
Differential Impedance		Z_{eDP}	90	100	110	Ω	

Note)

1. The measuring position is the connector of LCM and the test conditions are under 25℃, fv = 60Hz
2. The specified I_{CC} current and power consumption are under the V_{CC} = 3.3V , 25℃, fv = 60Hz condition and Mosaic pattern.



3. The V_{CC} rising time is same as the minimum of T1 at Power on sequence.



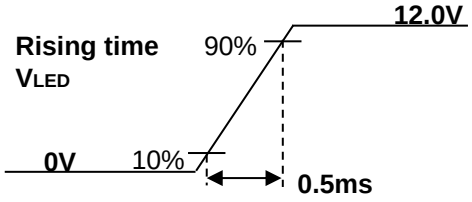
3-2. LED Backlight Electrical Characteristics

Table 3. LED B/L ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
LED Power Input Voltage		V_{LED}	5.0	12.0	21.0	V	1
LED Power Input Current		I_{LED}	-	246	250	mA	2
LED Power Consumption		P_{LED}	-	3.16	3.25	W	
LED Power Inrush Current		I_{LED_P}	-	-	1.5	A	3
PWM Duty Ratio			5	-	100	%	4
PWM resolution				10		Bit	5
PWM Jitter			0	-	0.05	%	6
PWM Frequency		F_{PWM}	200	-	2000	Hz	
PWM	High Level Voltage	V_{PWM_H}	2.5	-	3.6	V	
	Low Level Voltage	V_{PWM_L}	0	-	0.3	V	
LED_EN	High Voltage	$V_{LED\_EN\_H}$	2.5	-	3.6	V	
	Low Voltage	$V_{LED\_EN\_L}$	0	-	0.6	V	
Life Time			15,000	-	-	Hrs	8

Note)

1. The measuring position is the connector of LCM and the test conditions are under 25℃.
2. The current and power consumption with LED Driver are under the V_{LED} = 12.0V , 25℃, PWM Duty 100% and White pattern with the normal frame frequency operated(60Hz).
3. The V_{LED} rising time is same as the minimum of T13 at Power on sequence.

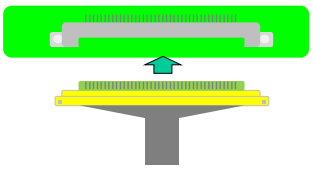


4. The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.
5. 10bit resolution means it's possible to change PWM duty by 0.1% step. (8bit operated by 0.4% step)
6. If Jitter of PWM is bigger than maximum, it may induce flickering.
7. This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
8. The life time is determined as the time at which brightness of LCD is 50% compare to that of minimum value specified in table 7. under general user condition.

3-3. Interface Connections

Table 4. MODULE CONNECTOR PIN CONFIGURATION (CN1)

Pin	Symbol	Description	Notes
1	NC	NC Reserved	
2	GND	High Speed Ground	
3	Lane1_N	Complement Signal Link Lane 1	
4	Lane1_P	True Signal Link Lane 1	
5	GND	High Speed Ground	
6	Lane0_N	Complement Signal Link Lane 0	
7	Lane0_P	True Signal Link Lane 0	
8	GND	High Speed Ground	
9	AUX_CH_P	True Signal Auxiliary Channel	
10	AUX_CH_N	Complement Signal Auxiliary Channel	
11	GND	High Speed Ground	
12	VCC	LCD logic and driver power	[Connector] LGC, GT05Q-40S-H10 or equivalent (40pin, 0.5pitch)
13	VCC	LCD logic and driver power	
14	NC	NC Reserved	
15	GND	LCD logic and driver ground	
16	GND	LCD logic and driver ground	
17	HPD	Built-In Self Test (active high)	
18	BL_GND	LED Backlight ground	[Connector pin arrangement] Pin 40 Pin 1
19	BL_GND	LED Backlight ground	
20	BL_GND	LED Backlight ground	
21	BL_GND	LED Backlight ground	
22	BL ENABLE	LED Backlight control on/off control	
23	BL PWM	System PWM signal input for dimming	
24	NC Reserved	Reserved for LCD manufacture's use	
25	NC Reserved	Reserved for LCD manufacture's use	
26	VLED	LED Backlight power (12V Typical)	
27	VLED	LED Backlight power (12V Typical)	
28	VLED	LED Backlight power (12V Typical)	[LGD P-Vcom using information] 1. Pin for P-Vcom : #24, #25 2. P-Vcom Address : 0101000x
29	VLED	LED Backlight power (12V Typical)	
30	NC Reserved	Reserved for LCD manufacture's use	
31	TP_DM	USB Negative Data (Touch)	
32	TP_DP	USB Positive Data (Touch)	
33	GND	Ground	
34	VTSP	Touch panel power supply(3.3V)	
35	VTSP	Touch panel power supply(3.3V)	
36	Touch_EN	Touch Enable (High: Enable[Pull-up 3.3V at LCM Side], Low : Disable)	
37	NC	I2C Clock (Touch), [NC for USB Input]	
38	NC	I2C Data (Touch), [NC for USB Input]	
39	NC	I2C Interrupt Signal (Touch), [NC for USB Input]	
40	NC	NC Reserved	



3-3-1. Input/output signal circuit

Figure1.HPD Output circuit is as below

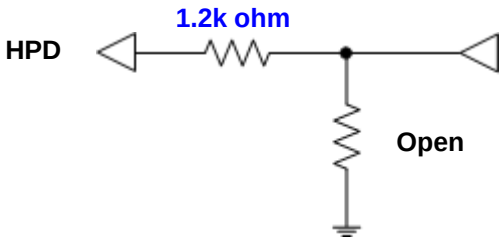


Figure2.BL PWM input circuit is as below

Figure3.BL Enable input circuit is as below

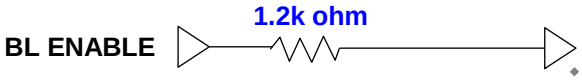


Figure4.BIST input circuit is as below

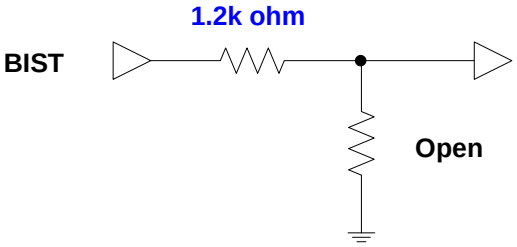
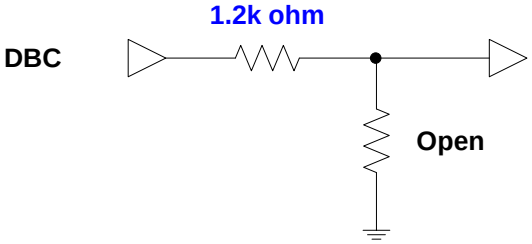
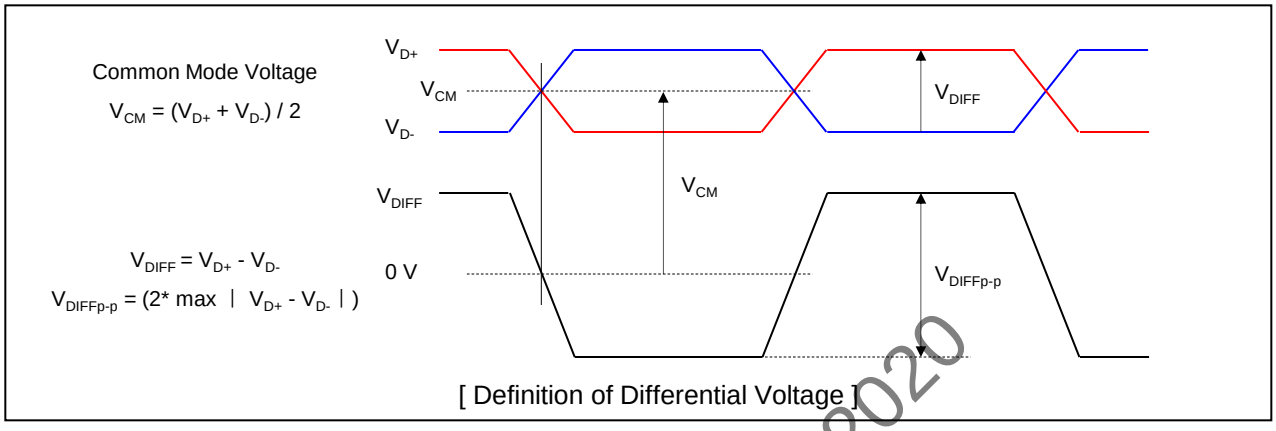


Figure5.DBC input circuit is as below



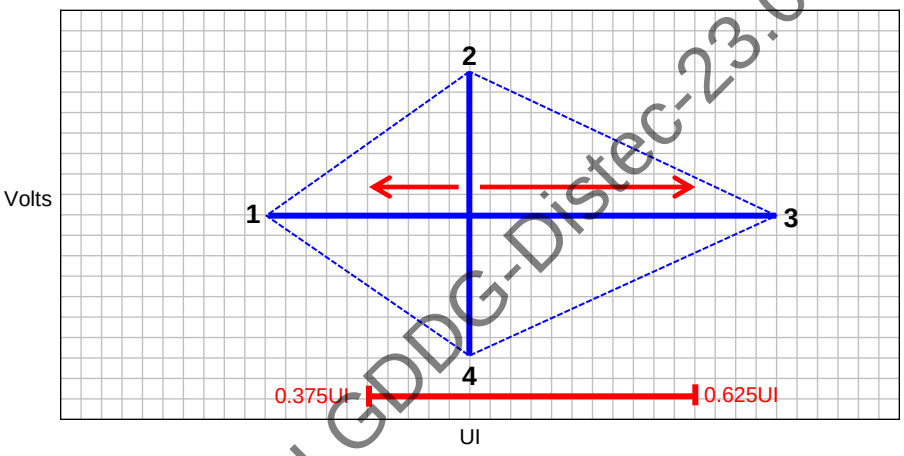
3-4. eDP Signal Timing Specifications

3-4-1. Definition of Differential Voltage



[Definition of Differential Voltage]

3-4-2. Main Link EYE Diagram



[EYE Mask at TP3_EQ/RX_EQ]

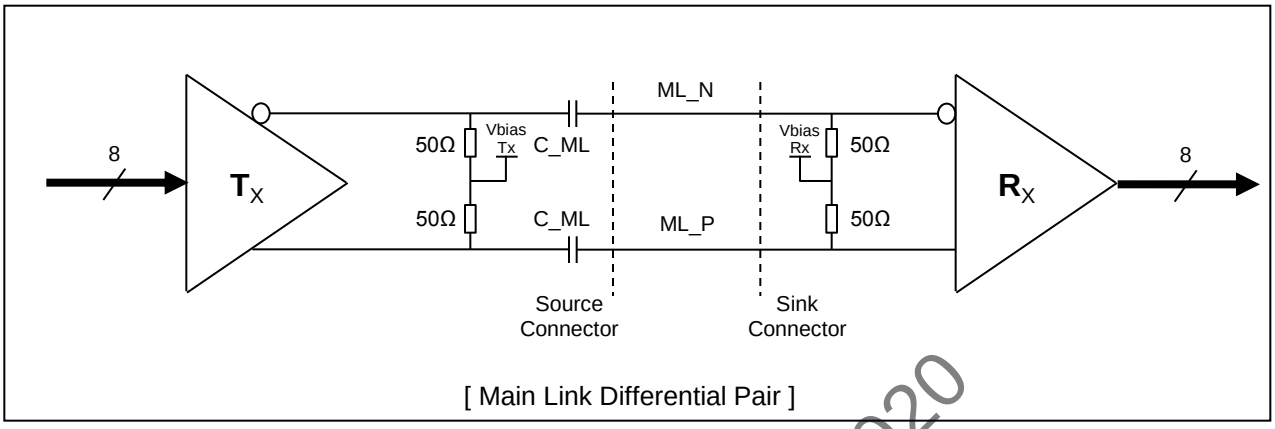
Point	Time(UI)	Voltage(V)
1	Any UI location (0mV)	0.000
2	0.375<point2<0.625	0.0375
3	Point1 + 0.5UI	0.000
4	0.375<point4<0.625	-0.0375

[eDP TP3_EQ EYE Mask Vertices]

Point	Time(UI)	Voltage(V)
1	Any UI location (0mV)	0.000
2	0.375<point2<0.625	0.035
3	Point1 + 0.45UI	0.000
4	0.375<point2<0.625	-0.035

[EYE Mask Vertices at embedded DP Sink Connector Pins]
[eDP RX_EQ EYE Mask Vertices]

3-4-3. eDP Main Link Signal

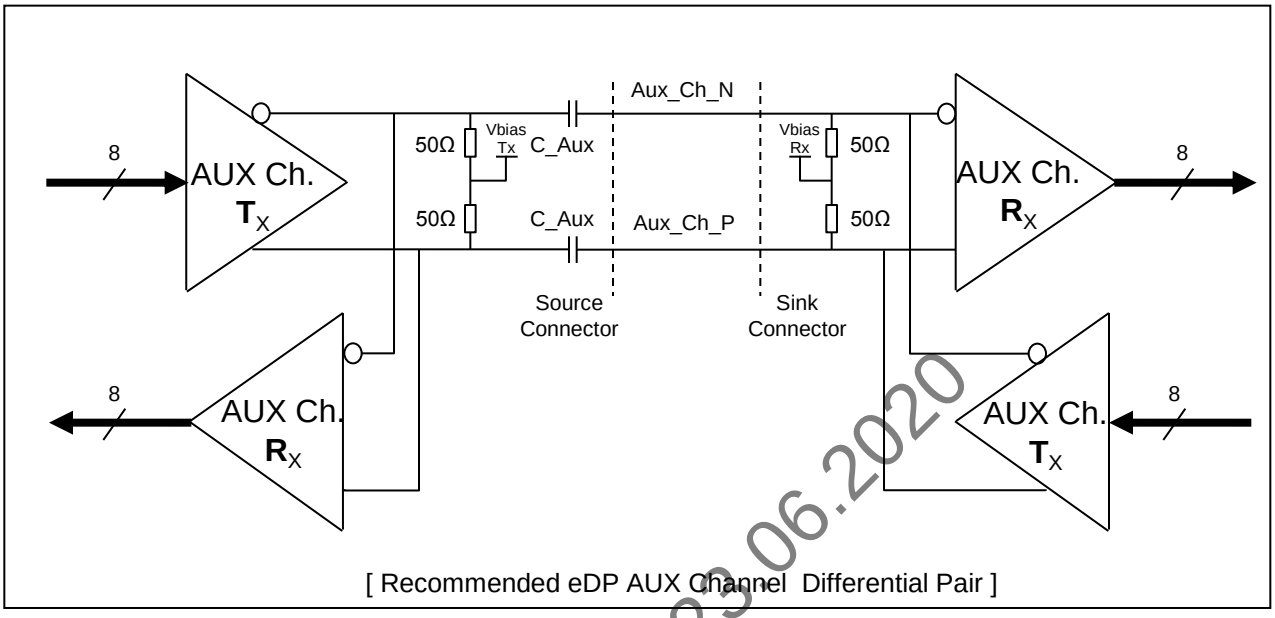


[Main Link Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval for high bit rate (2.7Gbps / lane)	UI_HBR	-	370	-	ps	
Unit Interval for reduced bit rate (1.62Gbps / lane)	UI_RBR	-	617	-	ps	
Link Clock Down Spreading	Amplitude	0	-	0.5	%	
	Frequency	30	-	33	kHz	
Differential peak-to-peak Voltage at Sink side connector	$V_{TX-DIFFp-p}$	75	-	-	mV	TP3_EQ
EYE width at Sink side connector	$T_{TX-EYE-CONN}$	0.5	-	-	UI	TP3_EQ
Differential peak-to-peak voltage at RX package pin	$V_{RX-DIFFp-p}$	70	-	-	mV	TP4_EQ
EYE width at RX package pin	$T_{RX-EYE-CONN}$	0.45	-	-	UI	TP4_EQ
Rx DC common mode voltage	$V_{RX\ CM}$	0	-	1.0	V	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

Note)
1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. In cabled embedded system, it is recommended the system designer ensure that EYE width and voltage are met at the sink side connector pins.

3-4-4. eDP AUX Channel Signal

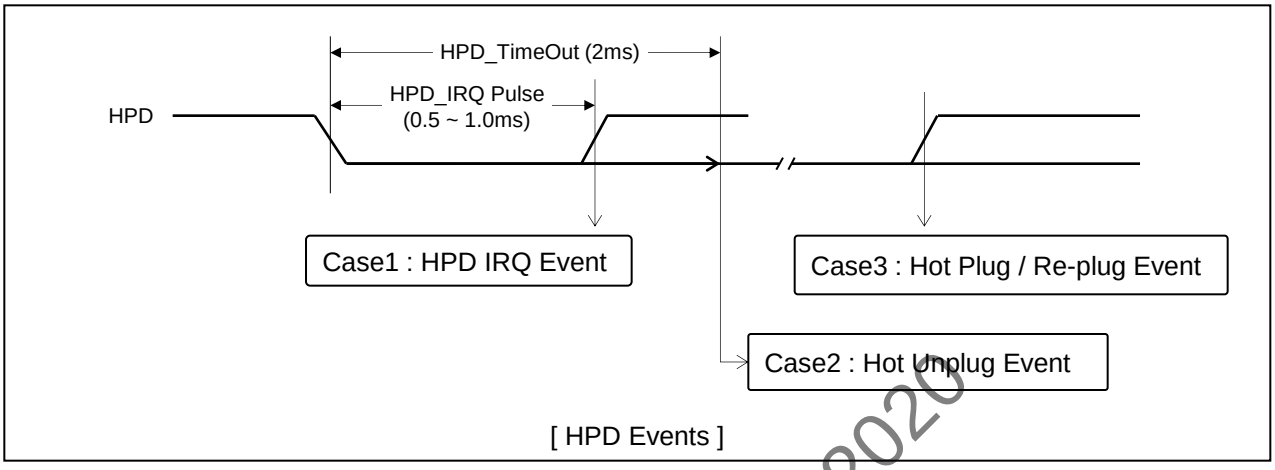


[Recommended eDP AUX Channel Differential Pair]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Unit Interval	UI	0.4	-	0.6	us	
AUX Jitter at Tx IC Package Pins	T_{jitter}	-	-	0.04	UI	Equal to 24ns
AUX Jitter at Rx IC Package Pins		-	-	0.05	UI	Equal to 30ns
AUX Peak-to-peak voltage at TX package pins (TP1)	$V_{AUX-DIFFp-p}$	0.18	0.20	1.38	V	
AUX Peak-to-peak voltage at TP3		0.14	-	1.36	V	
AUX EYE width at Connector Pins of Tx and Rx		0.98	-	-	UI	
AUX DC common mode voltage	V_{AUX-CM}	0	-	1.0	V	
AUX AC Coupling Capacitor	$C_{SOURCE-AUX}$	75		200	nF	Source side

Note)
1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. $V_{AUX-DIFFp-p} = 2^* | V_{AUXP} - V_{AUXN} |$

3-4-5. eDP HPD Signal



[HPD Events]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
HPD Voltage	HPD	2.25	-	3.6	V	Sink side Driving
Hot Plug Detection Threshold		2.0	-	-	V	Source side Detecting
Hot Unplug Detection Threshold		-	-	0.8	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1.0	ms	
HPD_TimeOut		2.0	-	-	ms	HPD Unplug Event

Note)
1. HPD IRQ : Sink device wants to notify the Source device that Sink's status has changed so it toggles HPD line, forcing the Source device to read its Link / Sink Receiver DPCD field via the AUX-CH
2. HPD Unplug : The Sink device is no longer attached to the Source device and the Source device may then disable its Main Link as a power saving mode
3. Plug / Re-plug : The Sink device is now attached to the Source device, forcing the Source device to read its Receiver capabilities and Link / Sink status Receiver DPCD fields via the AUX-CH

3-5. Signal Timing Specifications

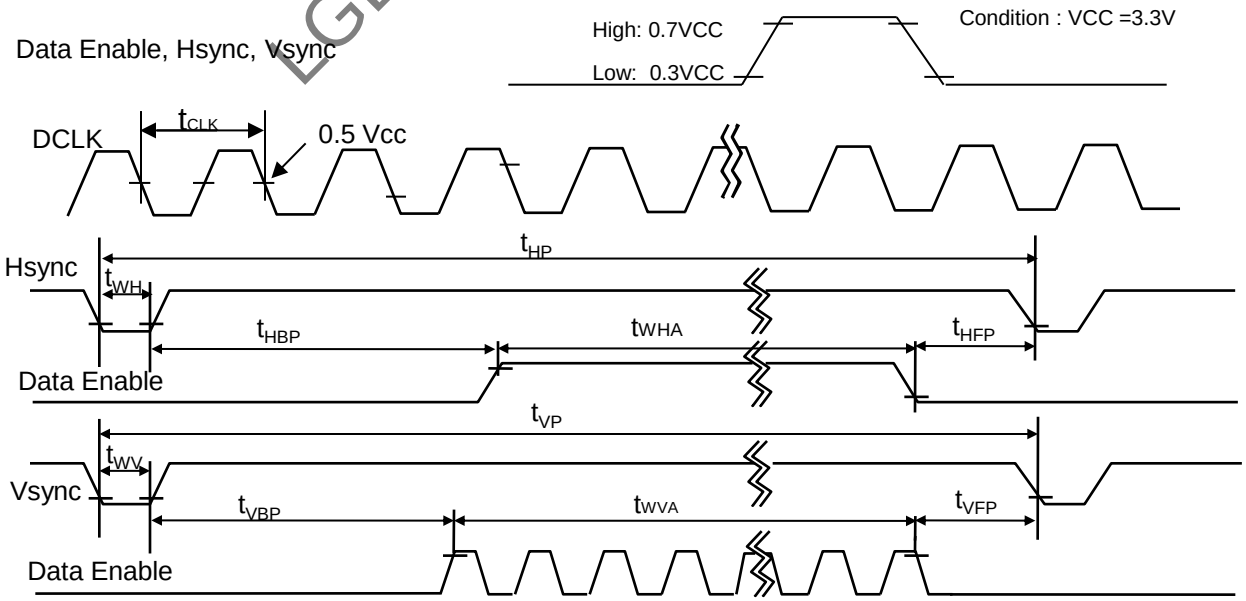
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of eDP Tx/Rx for its proper operation.

Table 4. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	-	138.65	-	MHz	
Hsync	Period	t_{HP}	2078	2080	2082	t_{CLK}	
	Width	t_{WH}	32	32	32		
	Width-Active	t_{WHA}	1920				
Vsync	Period	t_{VP}	1108	1111	1114	t_{HP}	
	Width	t_{WV}	5	5	5		
	Width-Active	t_{WVA}	1080				
Data Enable	Horizontal back porch	t_{HBP}	78	80	82	t_{CLK}	
	Horizontal front porch	t_{HFP}	48	48	48		
	Vertical back porch	t_{VBP}	20	23	24	t_{HP}	
	Vertical front porch	t_{VFP}	3	3	5		

Notice. all reliabilities are specified for timing specification based on refresh rate of 60Hz. However, LP156WFD has a good actual performance even at lower refresh rate (e.g. 40Hz or 50Hz) for power saving Mode, whereas LP156WFD is secured only for function under lower refresh rate. 60Hz at Normal mode, 50Hz, 40Hz at Power save mode. Don't care Flicker level, Touch Report Rate (Power save mode).

3-6. Signal Timing Waveforms



3-7. Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

Color		Input Color Data																	
		RED						GREEN						BLUE					
		MSB					LSB	MSB					LSB	MSB					LSB
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	…	…						…						…					
	RED (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	...	...						...						...					
	GREEN (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	GREEN (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
BLUE	BLUE (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	…	…						…						…					
	BLUE (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	BLUE (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

3-8. Power Sequence

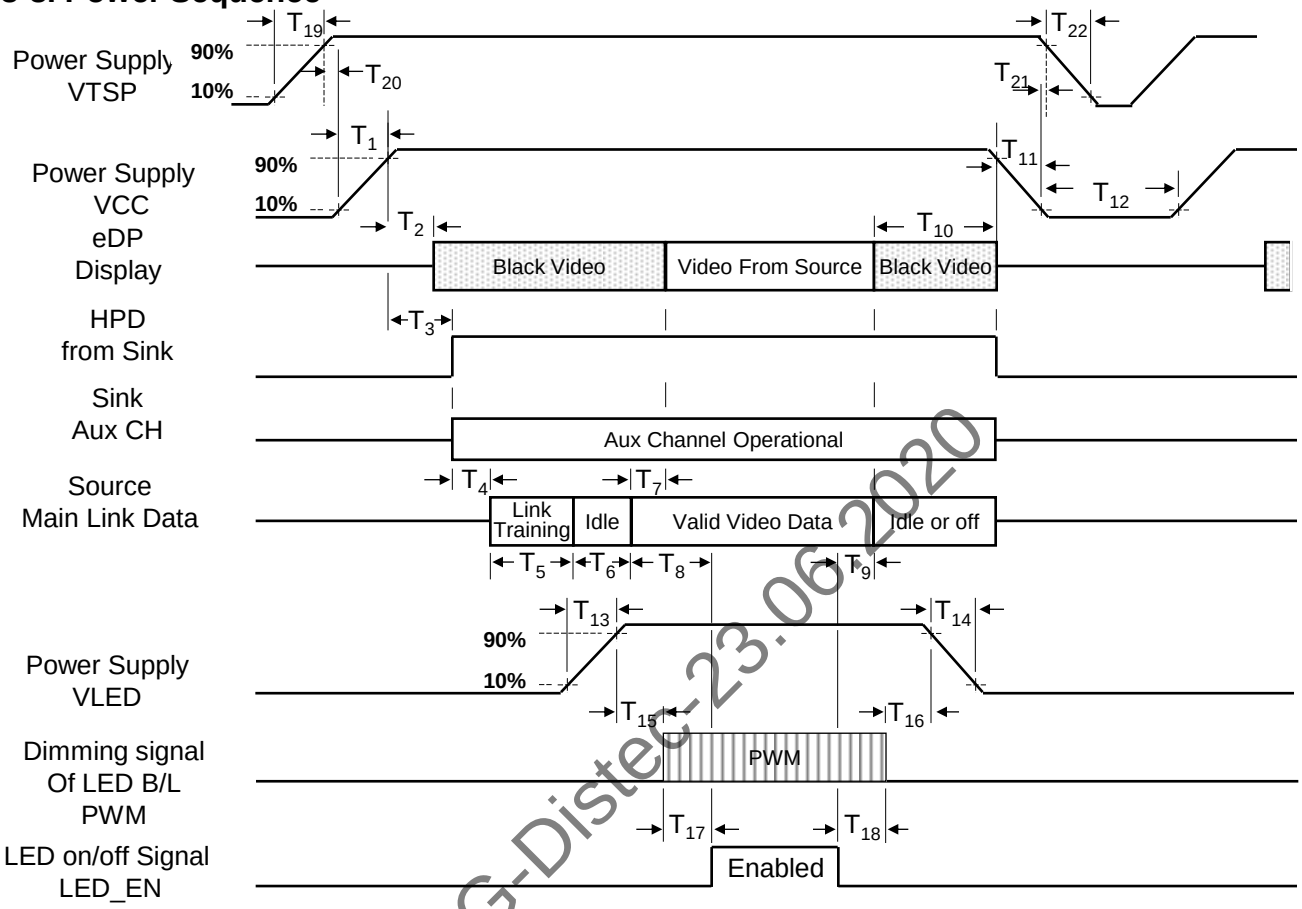


Table 6. POWER SEQUENCE TABLE

Symbol	Required By	Limits		Units	Notes
		Min	Max		
T_1	Source	0.5	10	ms	-
T_2	Sink	0	200	ms	-
T_3	Sink	0	200	ms	-
T_4	Source	-	-	ms	-
T_5	Source	-	-	ms	-
T_6	Source	-	-	ms	-
T_7	Sink	0	50	ms	-
T_8	Source	-	-	ms	5
T_9	Source	-	-	ms	6
T_{10}	Source	-	500	ms	
T_{11}	Source	-	60	ms	-

Symbol	Required By	Limits		Units	Notes
		Min	Max		
T_{12}	Source	500	-	ms	VESA recommend Min 500ms
T_{13}	Source	0.5	10	ms	-
T_{14}	Source	0.5	10	ms	-
T_{15}	Source	10	-	ms	-
T_{16}	Source	10	-	ms	-
T_{17}	Source	0	-	ms	-
T_{18}	Source	0	-	ms	-
T_{19}	Source	0.5	10	ms	-
T_{20}	Source	70	-	ms	-
T_{21}	Source	0	-	ms	-
T_{22}	Source	0.5	10	ms	-

Note) 1. Do not insert the mating cable when system turn on.
2. Valid Data have to meet “3-3. eDP Signal Timing Specifications”
3. Video Signal, LED_EN and PWM need to be on pull-down condition on invalid status.
4. LGD recommend the rising sequence of VLED after the Vcc and valid status of Video Signal turn on.
5. Driving signal of B/L must be “On” after normal video signal (Normal operating data from source) input.
6. B/L driving must be “Off” before normal signal (Normal operating data from source) finish.

4. Touch Specifications

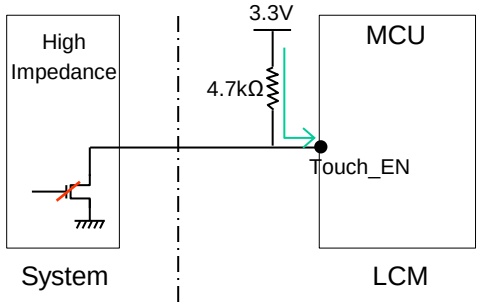
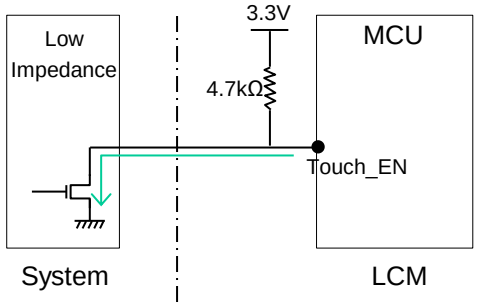
4-1. General Specifications

The contents provide general characteristics for the model LP156WFD.

	Item		Spec	Notes
General Specification	System		Self Capacitive type	
	Multi Touch Points		10 points	
	Active touch area		Same as LCD A/A	
	Sensor	Type.	Advanced In-Cell Touch	
		Sensor Channel Pitch	4.302mm (X) x 5.38mm(Y)	
	Touch IC Information	IC	MIT-410	Melfas
		Firmware	01.02	
		PID	9004	
		VID	1FD2	
	Number of Sensor Channel		80ea (X) x 36ea (Y)	
	Interface		USB	

4-2. Electrical Characteristics

Item	Symbol		Value			unit	Notes
			Min.	Typ.	Max		
Input Logical Voltage	TP_EN	VIH	2.3	3.3	3.6	V	
		VIL	-0.5	0	0.6	V	
Pull-up resistance (system side)	TP_EN	-	-	N/A	-	kΩ	System Open drain port LCM side Pull-up (3.3V)

	When impedance is high,	When impedance is low
Recommend Circuit (Open drain)	▪ Touch_EN is high(3.3V) and enable 	▪ Touch_EN is low(GND) and disable 

4-3. Power Sequence for Touch

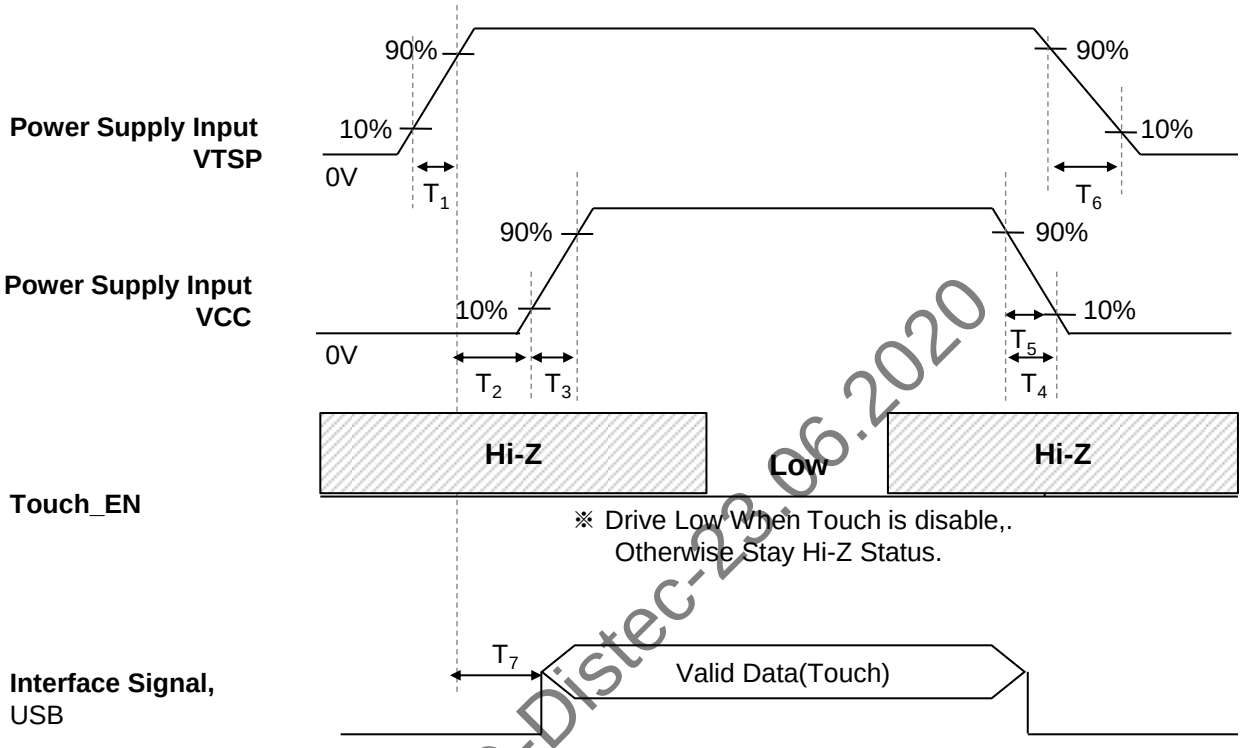


Table 9. POWER SEQUENCE TABLE

Parameter	Value			Units	Notes
	Min.	Typ.	Max.		
T_1	0.5	-	10	ms	
T_2	150	-	-	ms	
T_3	0.5	-	10	ms	
T_4	0.5	-	60	ms	
T_5	0	-	-	ms	
T_6	0.5	-	30	ms	
T_7	1100	-	-	ms	

5. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

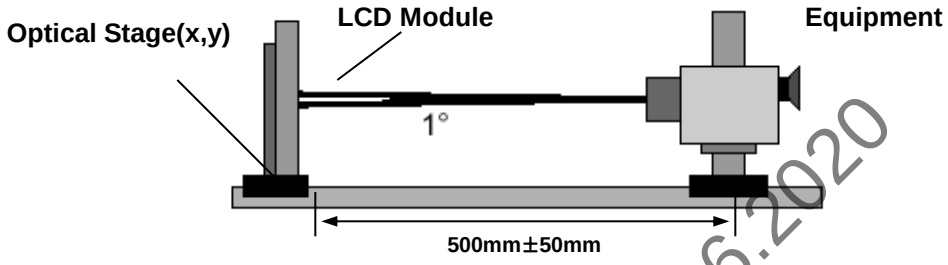


Table 7. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz

Parameter		Symbol	Values			Units	Notes
			Min	Typ	Max		
Contrast Ratio		CR	500	700	-		1
Surface Luminance, white		L_{WH}	213	250	-	cd/m²	2
Luminance Variation		$\delta_{WHITE\ (5P)}$	-	1.2	1.4	-	3
		$\delta_{WHITE(13P)}$	-	1.4	1.6		
Response Time		Tr + Tf	-	25	35	ms	4
Color Coordinates	RED	Rx	Typical - 0.03	0.590	Typical + 0.03		5
		Ry		0.370			
	GREEN	Gx		0.350			
		Gy		0.555			
	BLUE	Bx		0.155			
		By		0.110			
	WHITE	Wx		0.313			
		Wy		0.329			
Viewing Angle	x axis, right(Φ=0°)	Θr	80	85	-	Degree	6
	x axis, left (Φ=180°)	Θl	80	85	-		
	y axis, up (Φ=90°)	Θu	80	85	-		
	y axis, down (Φ=270°)	Θd	80	85	-		
Gray Scale							7

Note)

1. It should be measured in the center of screen(1 Point). Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio(1 Point)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 2.

$$L_{WH} = \text{Average(1,2, … 5 Point)}$$

3. The variation in surface luminance , The panel total variation (δ WHITE) is determined by measuring N at each test position 1 through 13 and then defined as following numerical formula. For more information see FIG 2.

$$\delta \text{ WHITE (5P)} = \frac{\text{Maximum (1,2, … 5 Point)}}{\text{Minimum (1,2, … 5 Point)}} \qquad \delta \text{ WHITE (13P)} = \frac{\text{Maximum (1,2, … 13 Point)}}{\text{Minimum (1,2, … 13 Point)}}$$

4. Response time is the time required for the display to transition from black to white (rise time, Tr) and from white to black (falling time, Tf). For additional information see FIG 3.

5. It should be measured in the center of screen (1Point).

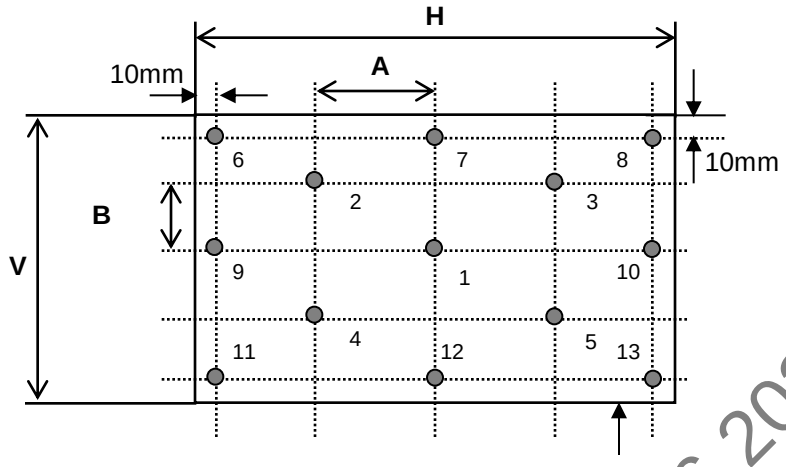
6. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

7. Gray scale specification

Gray Level	Luminance [%] (Typ)
L0	0.07
L7	0.80
L15	4.25
L23	10.90
L31	21.01
L39	34.82
L47	52.49
L55	74.17
L63	100

FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>



H,V : ACTIVE AREA
A : H/4 mm
B : V/4 mm
POINTS: 13 POINTS

FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

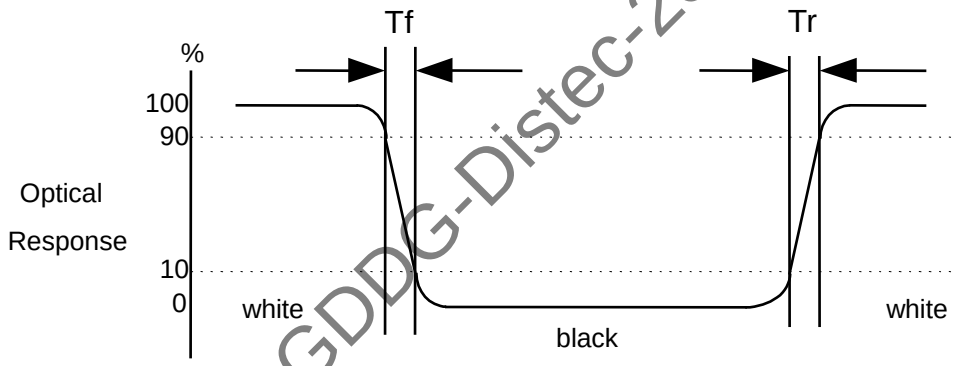
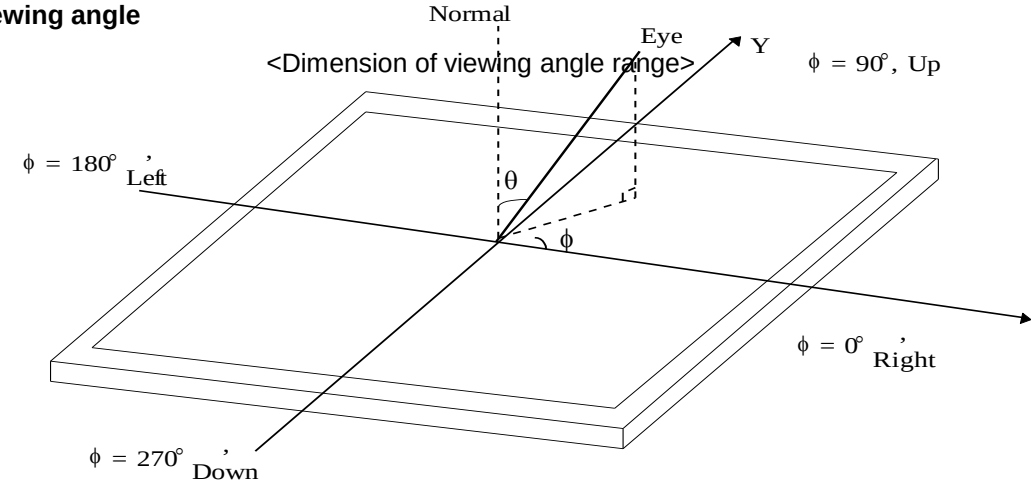


FIG. 4 Viewing angle

<Dimension of viewing angle range>



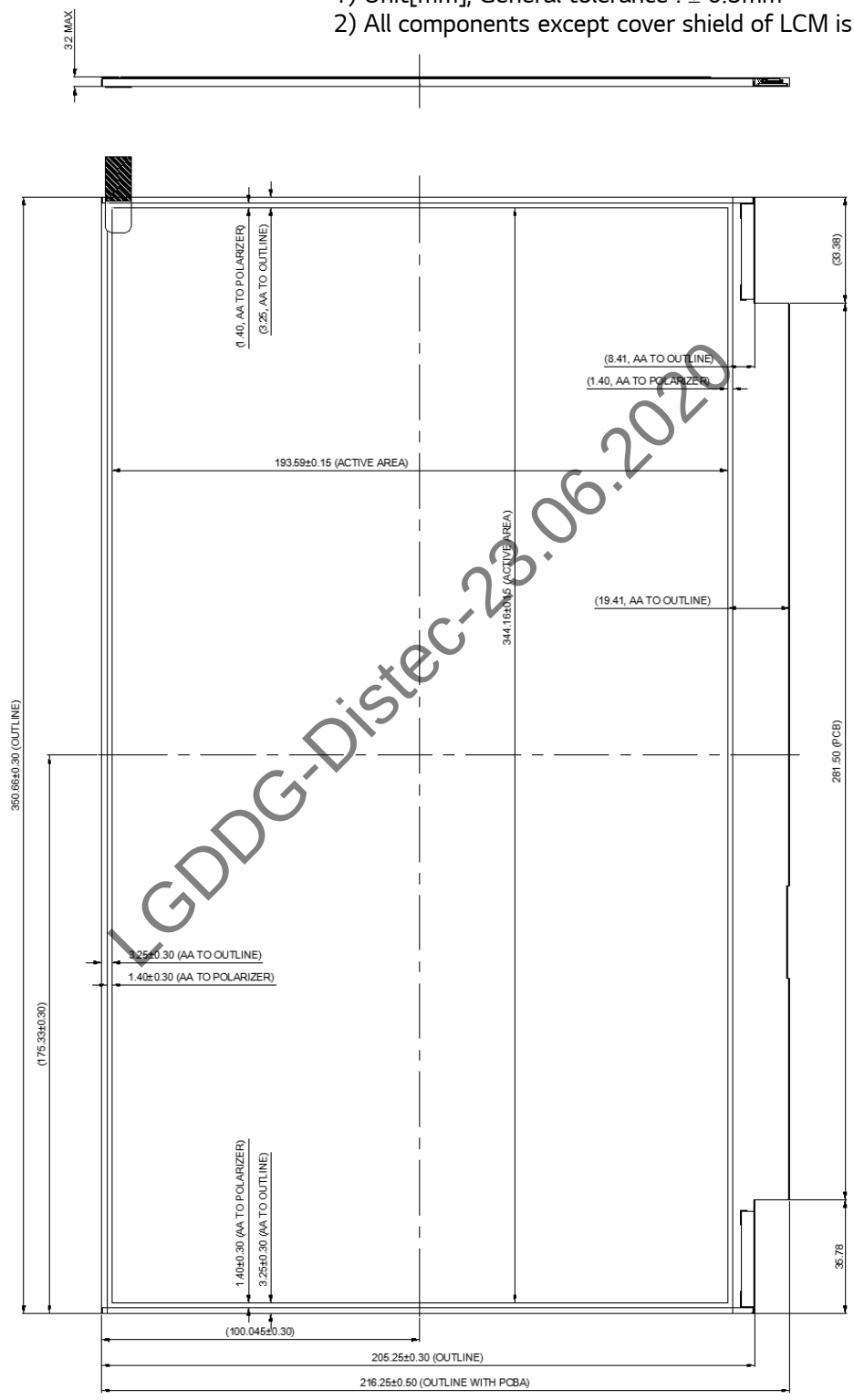
6. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP156WFD. In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	350.66 ± 0.3 mm
	Vertical	216.25 ± 0.5 mm (with PCB)
	Thickness (Max.)	3.2 mm (with PCB)
Upper Polarizer Dimension	Horizontal	346.95 ± 0.2 mm
	Vertical	196.39 ± 0.2 mm
Active Display Area	Horizontal	344.16 ± 0.15 mm
	Vertical	193.59 ± 0.15 mm
Weight	380g (Max.)	
Surface Treatment	Anti Glare treatment of the front polarizer	

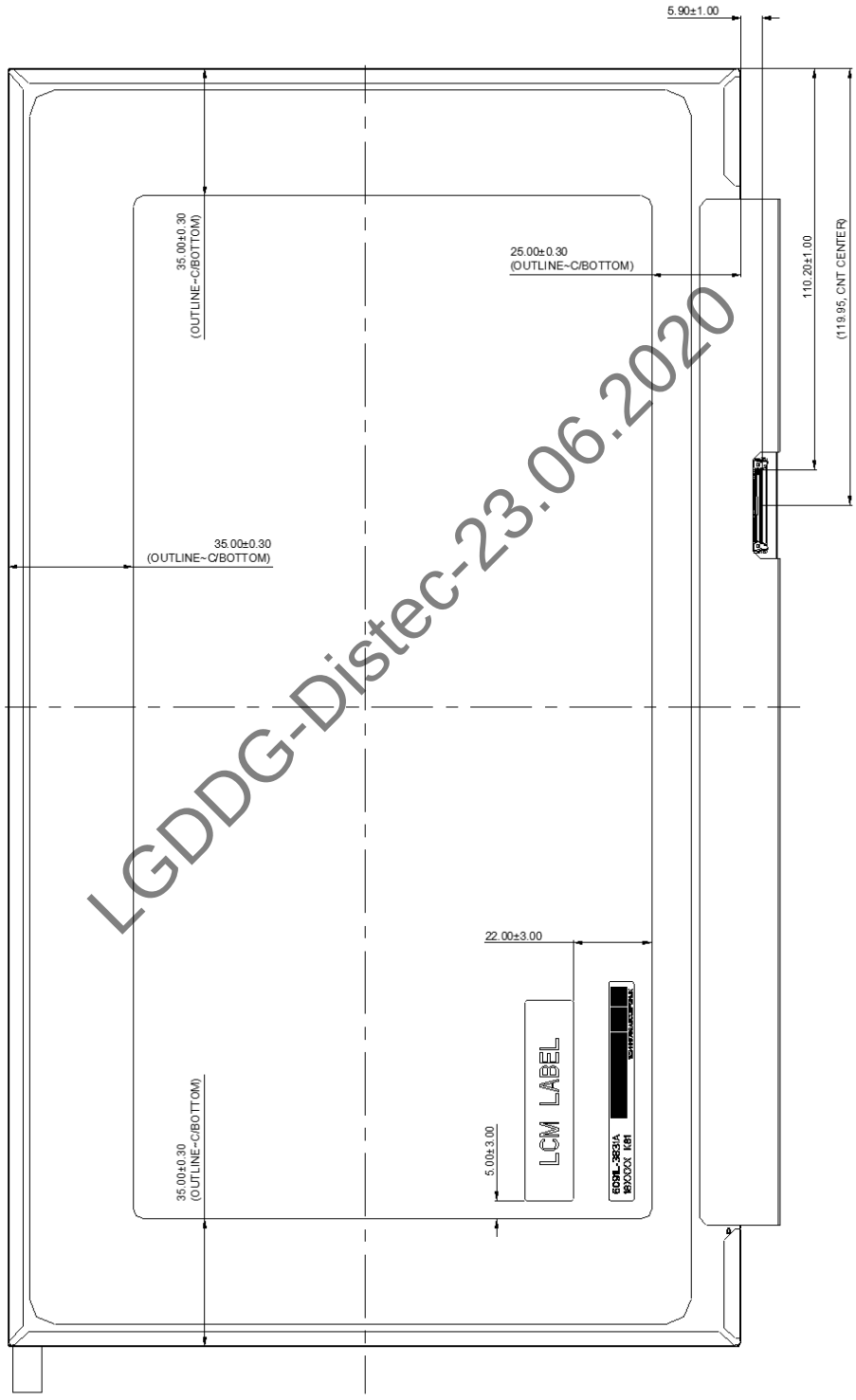
<FRONT VIEW>

Notes (Measurement method refer to the Appendix D)
1) Unit[mm], General tolerance : ± 0.5mm
2) All components except cover shield of LCM is under upper POL.



<REAR VIEW>

Notes
1) Unit[mm], General tolerance : ± 0.5mm
2) LCM Label Information refer to the page 27.



7. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Random, 1.0Grms, 10 ~ 300Hz(PSD 0.0035) 3 axis, 30min/axis
6	Shock test (non-operating)	- No functional or cosmetic defects following a shock to all 6 sides delivering at least 180 G in a half sine pulse no longer than 2 ms to the display module - No functional defects following a shock delivering at least 200 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr
8	ESD	± 8kV for contact discharge ± 15kV for air discharge

[Result Evaluation Criteria]

1. Comparing the initial functional FOS status, there should be no major change which might affect the practical display function when the display reliability test is conducted.

2. After conduct reliability tests, LGD guarantees only functional FOS quality.

3. In the Reliability Test, Confirm performance after leaving in room temp.

4. In the standard condition, there shall be no practical problems that may affect the display function 24 hours later after reliability test. After the reliability test, we can guarantee the product only when the corrosion is causing its malfunction. The corrosion causing no functional defect can not be guaranteed.

8. International Standards

8-1. Safety

a) UL 60950-1, Underwriters Laboratories Inc.
Information Technology Equipment - Safety - Part 1 : General Requirements.
b) CAN/CSA-C22.2 No. 60950-1-07, Canadian Standards Association.
Information Technology Equipment - Safety - Part 1 : General Requirements.
c) EN 60950-1, European Committee for Electro technical Standardization (CENELEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.
d) IEC 60950-1, The International Electro technical Commission (IEC).
Information Technology Equipment - Safety - Part 1 : General Requirements

8-2. Environment

a) RoHS, Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011

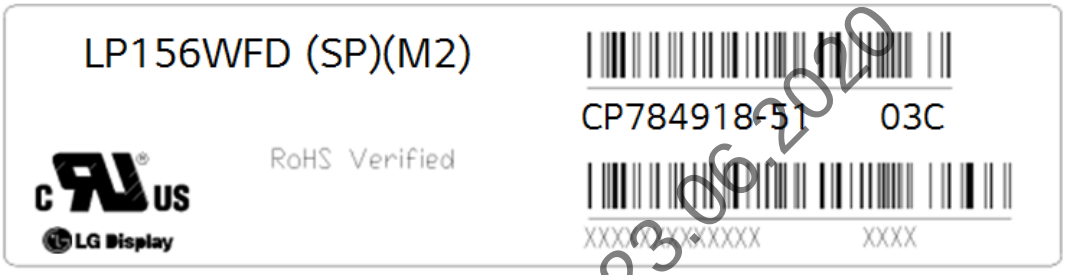
9. Packing

9-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.



Note

1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

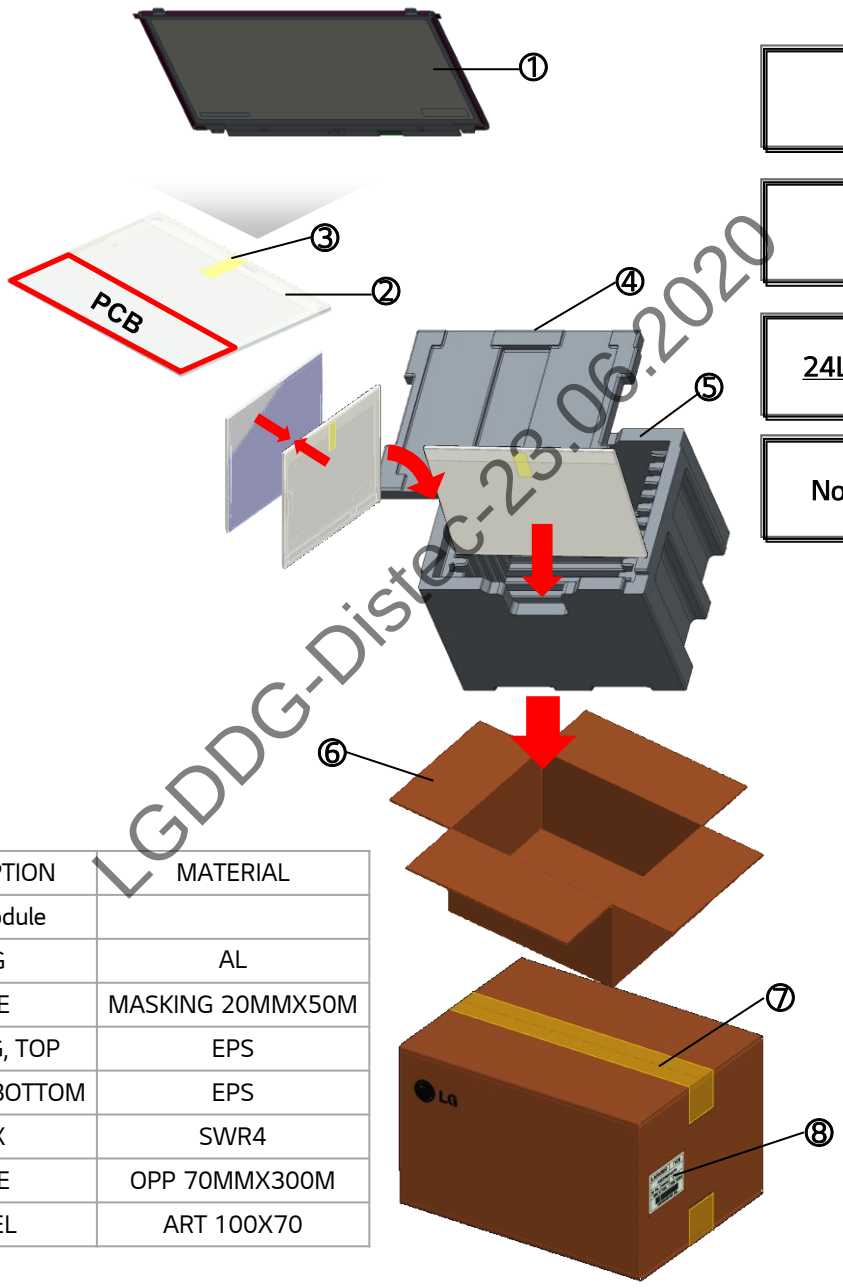
Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

9-2. Packing Form

a) Package quantity in one box : 24ea

b) Box Size : 478 x 365 x 244[mm]

9-3. Packing Assembly



1 LCM / 1 Bag

2 LCM / 1 Slot

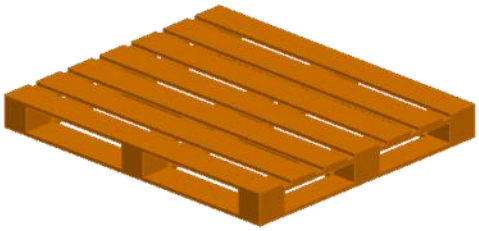
24LCM/Box = 12 Slot

No silica gel in the box

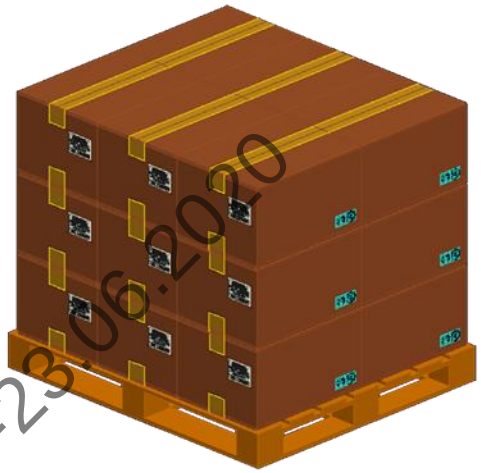
NO.	DESCRIPTION	MATERIAL
1	LCD Module	
2	BAG	AL
3	TAPE	MASKING 20MMX50M
4	PACKING, TOP	EPS
5	PACKING, BOTTOM	EPS
6	BOX	SWR4
7	TAPE	OPP 70MMX300M
8	LABEL	ART 100X70

9-3. Packing Assembly (Pallet)

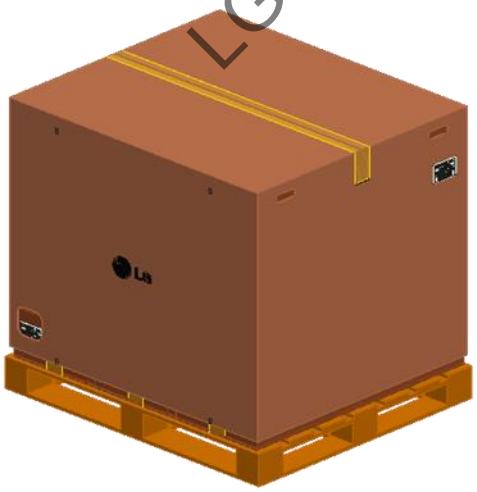
1. Pallet Ready



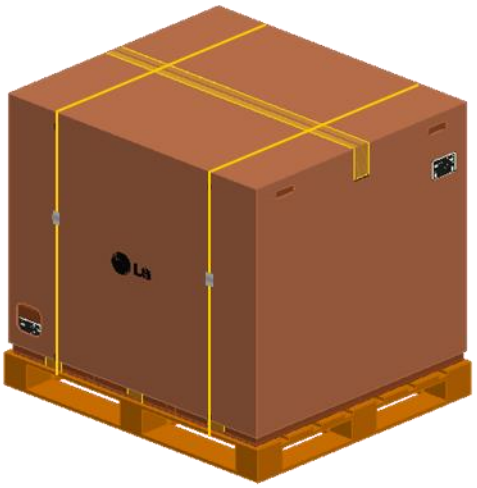
2. 3 x 2 x 3 Box Pattern



3. Angle Packing & Taping



4. Banding



10. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

10-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

10-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

10-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

10-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

10-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

10-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

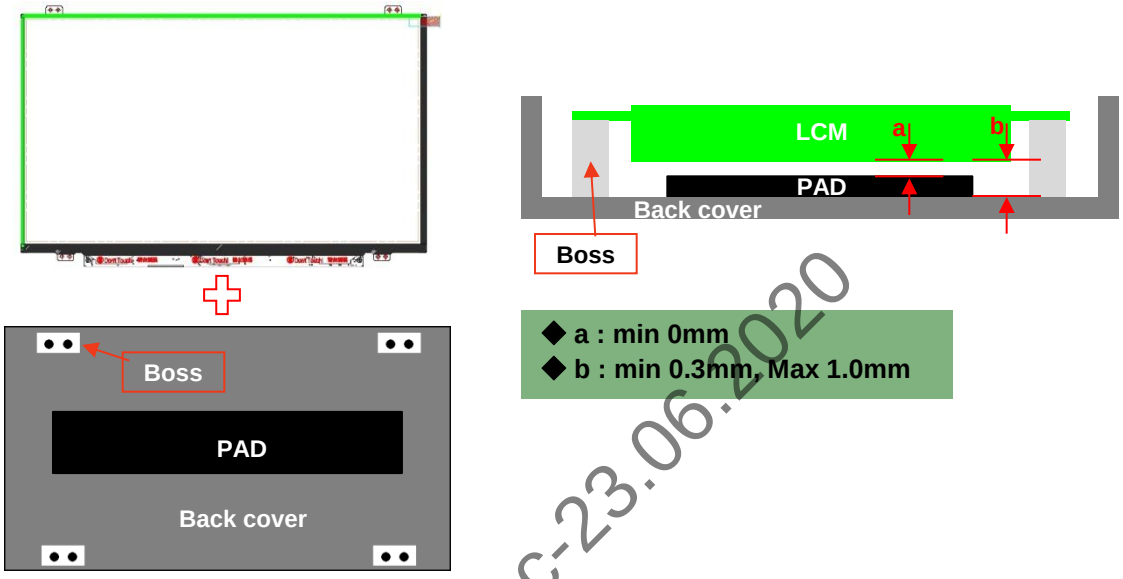
(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

10-7. THE LGD QA RESPONSIBILITY WILL BE AVOIDED IN CASE OF BELOW

(1) When the customer attaches cover glass on LCM without Supplier's approval.
(3) When the LCMs were repaired by 3rd party without Supplier's approval.
(4) When the LCMs were treated like Disassemble and Rework by the Customer and/or Customer's representatives without supplier's approval.

APPENDIX A. LGD Proposal for system cover design

1	**Gap check for securing the enough gap between LCM and System back cover.**

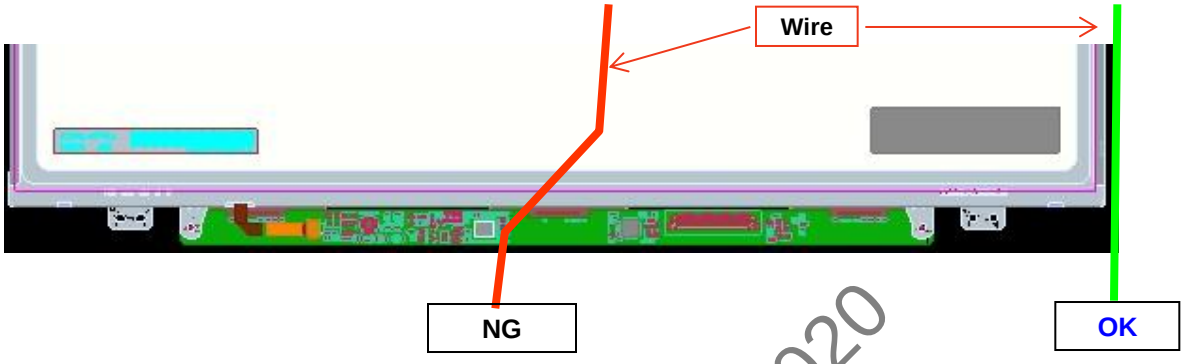


Define	1. Rear side of LCM is sensitive against external stress, and previous check about interference is highly needed.
	2. In case there is something from system cover comes into the boundary above, mechanical interference may cause the FOS defects. (e.g.. Ripple, White spot..)
2	**Check if antenna cable is sufficiently apart from T-CON of LCD Module.**

Define	If system antenna is overlapped with T-CON, It might be cause the noise

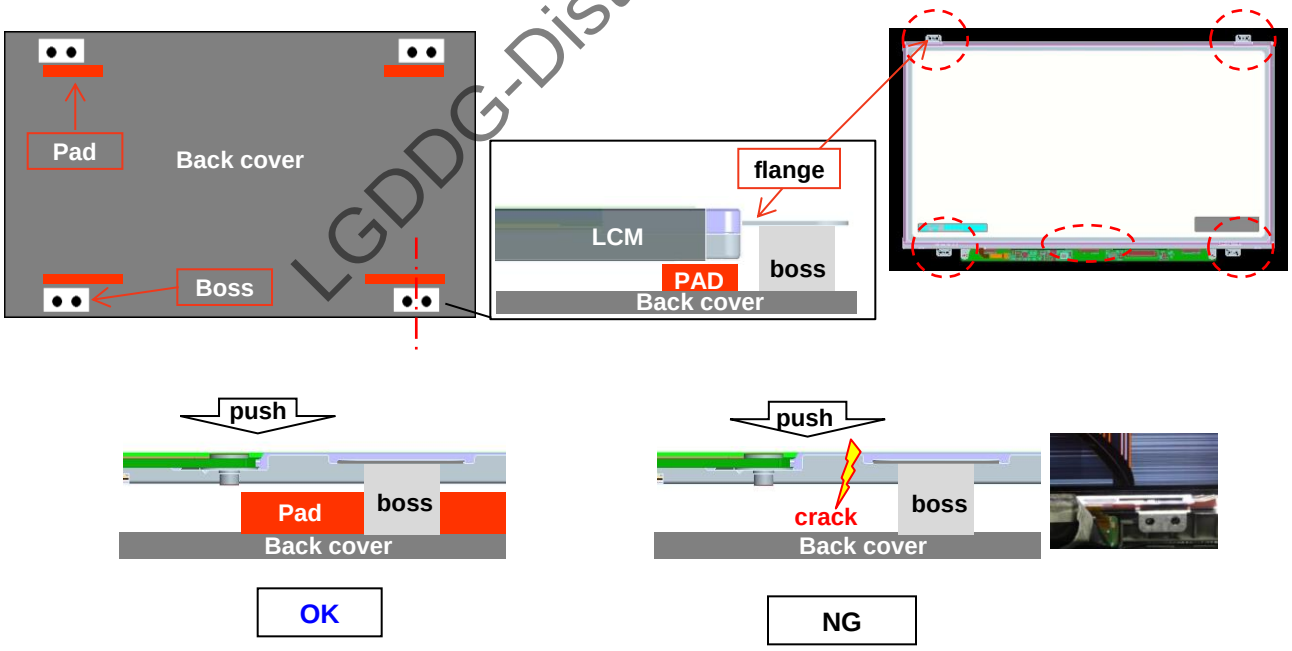
APPENDIX A. LGD Proposal for system cover design

3	**Checking the path of the System wire**



Define	1. If Wire path overlapped with LCM, it is happened white spot. COF problem, etc.
	2. OK ➔ Wire path design to system side. NG ➔ Wire path overlapped with LCM.

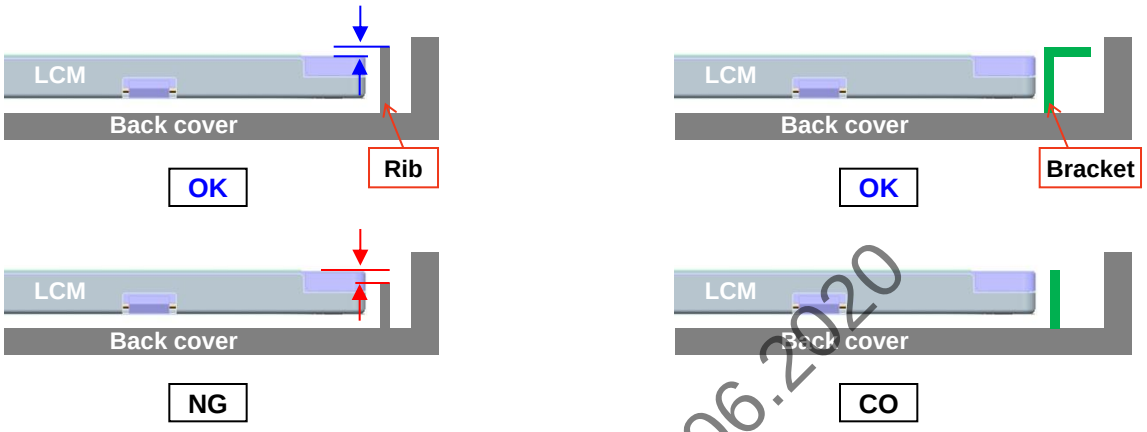
4	**Add pad to Prevent panel crack against external load (push)**



Define	1. At flat type LCM, panel is easily cracked at flange area during push, assemble.
	2. Add pad, it prevent panel crack

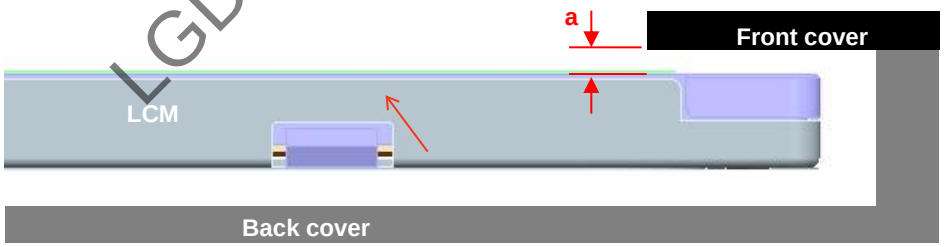
APPENDIX A. LGD Proposal for system cover design

5	**Check the rib or Bracket on back cover**



Define	1.It is necessary that the height of back cover rib or bracket is higher than LCM height. It can prevent direct compression of panel at LCM edge.
	2.”¬” shape bracket is stronger than “I” shape one.

6	**Check the gap between front cover and LCM (glass)**

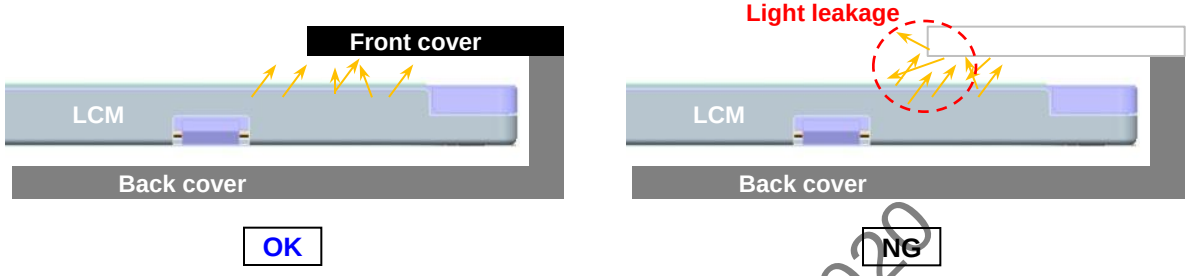


[OK] a ≥ 0.3mm
[CO] 0.3mm ≥ a ≥ 0.1mm
[NG] a ≤ 0.1mm

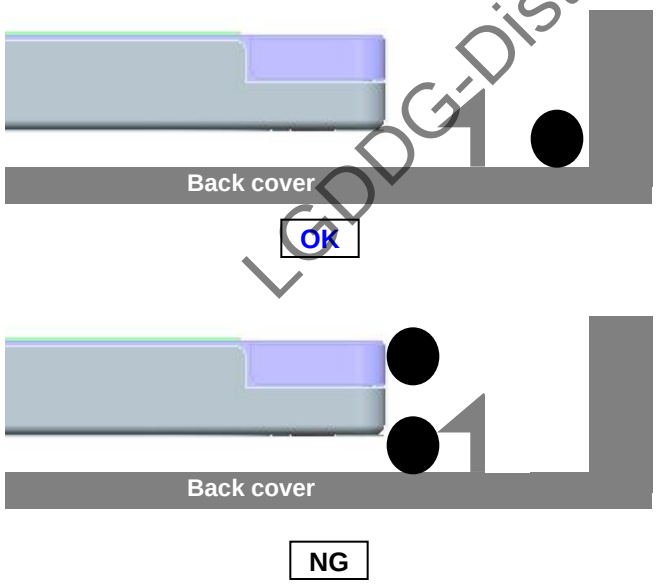
Define	Ripple can be happened by little gap between glass and front cover.

APPENDIX A. LGD Proposal for system cover design

7	**Check the rib or Bracket on back cover**



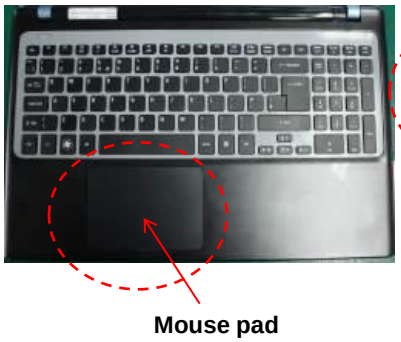
Define	1.If it is possible, shrink to apply front cover of white color.
	2. White color can caused light leakage
8	**Check the wire position(path)**



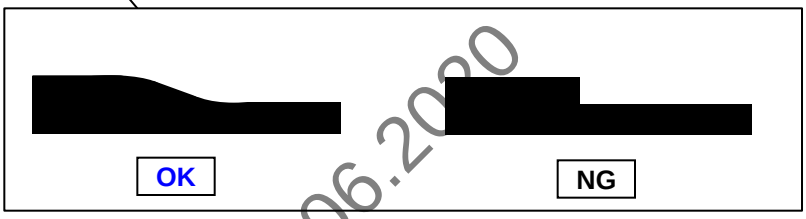
Define	1. It is necessary that wire is posited out of hook, not posited near hook,.
	2. If wire is posited near hook, it can be happened assemble error and panel crack during assemble front cover

APPENDIX A. LGD Proposal for system cover design

9	**Check mouse pad (touch pad) depth and shape of edge**

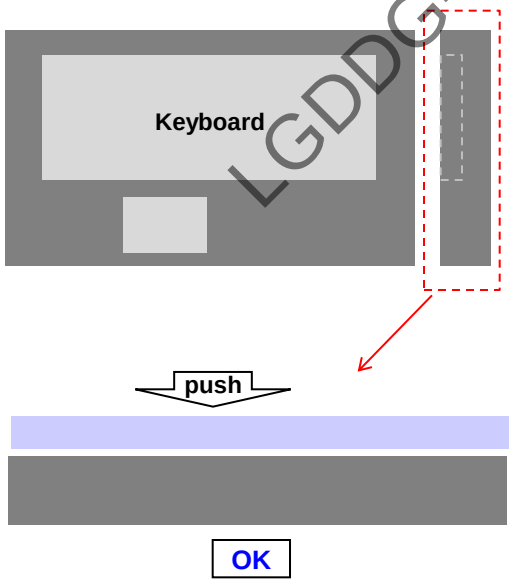


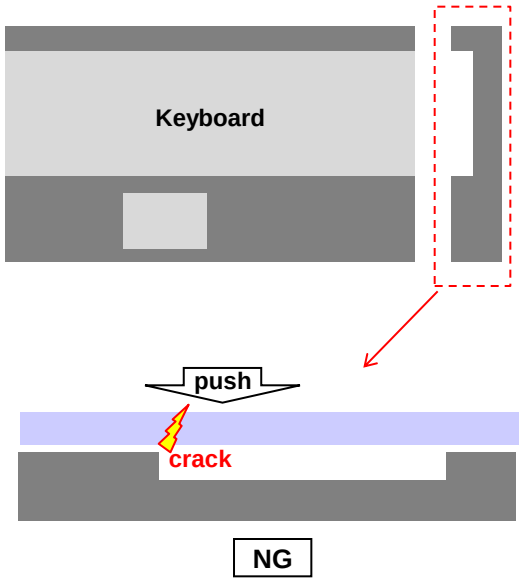
[OK] a ≤ 0.3mm
[CO] 0.5mm ≥ a ≥ 0.3mm
[NG] a ≥ 0.5mm



Define	1.Mouse pad step is deep, it is caused panel crack by external load.
	2. The edge shape must be smooth.

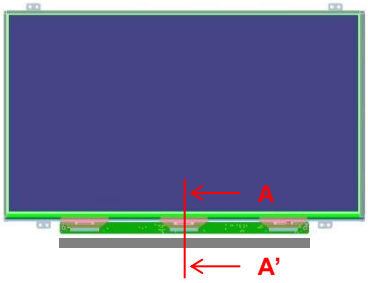
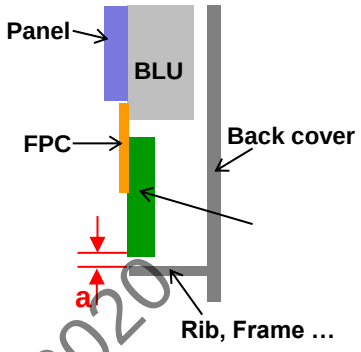
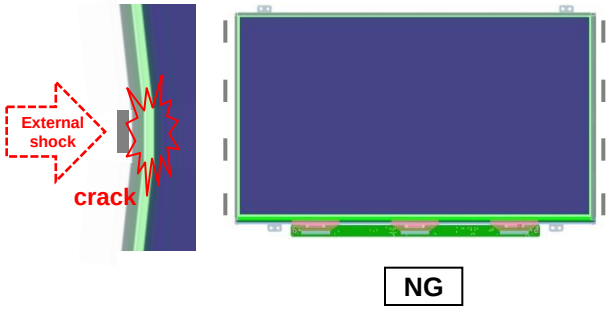
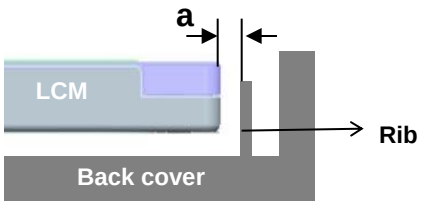
10	**Check the step of keyboard area**





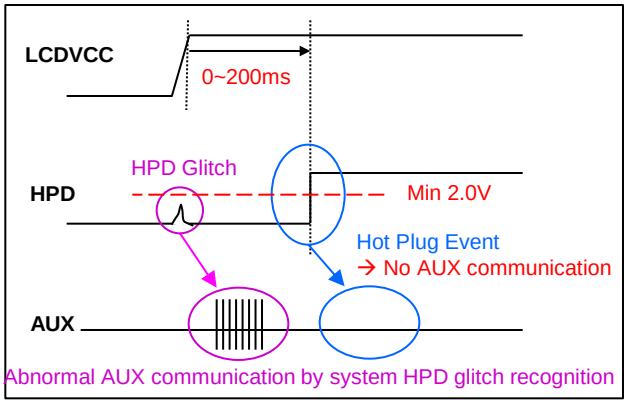
Define	The step of keyboard at the side edge of main body, it is caused panel crack

APPENDIX A. LGD Proposal for system cover design

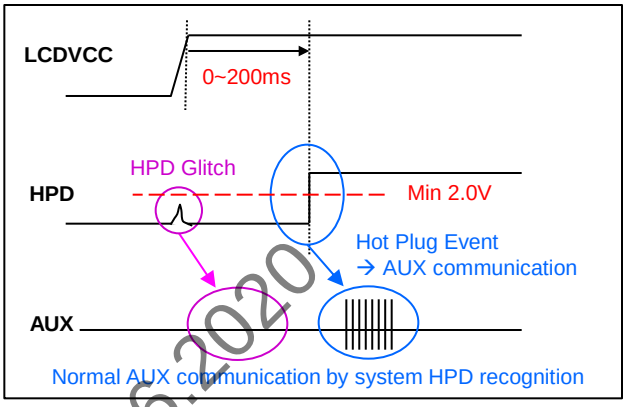
11	Check the gap [PCB ~ system]
	 **a ≥ 0.5mm [at max dimension of design]** **a ≥ 1.0mm [at typical dimension of design]** 
Define	1. Gap is too small, FPC is easily cracked by interference and repetitive bending. (circuit is opened) . 2. Gap is must be kept more than 0.5mm(max dim.) and 1.0mm(typ dim.) .
12	**System rib (on A cover)**
	 OK  NG  **a ≥ 0.5mm [at max dimension of design]** **a ≥ 1.0mm [at typical dimension of design]**
Define	1. Gap is too small and rib is too short, panel is easily cracked by external stress. 2. Gap is must be kept more than 0.5mm(max dim.) and 1.0mm(typ dim.) . 3. The figure of rib is continuous or fully long.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

1	HPD Signal recognition



[Abnormal Communication By HPD Glitch]

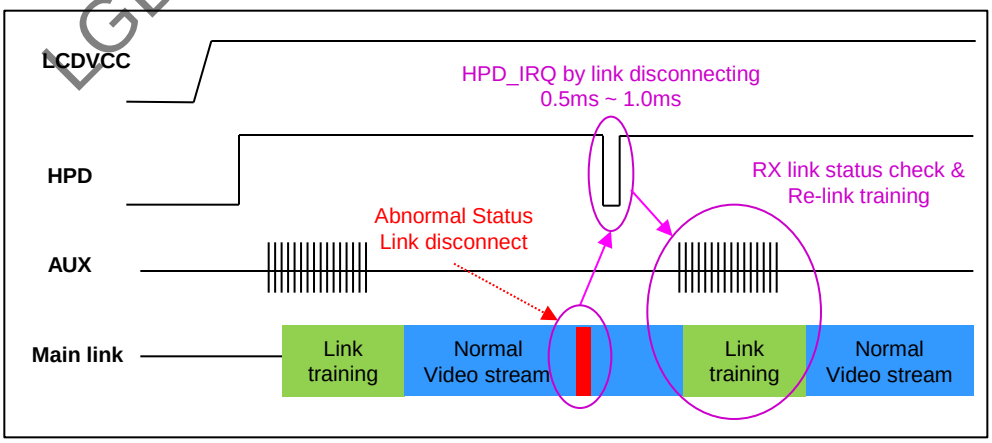


[Normal Communication By HPD Signal]

Define	1. Hot Plug Detection (HPD) Threshold level of Source Device is minimum 2.0V
	2. HPD Unplug : HPD pulse stays low longer than 2ms. DP Tx shall wait for HPD signal to go high again.
	3. "HPD High" is confirmed only after HPD has been asserted continuously for 100msec.

2	IRQ (Interrupt Request) HPD Pulse Definition

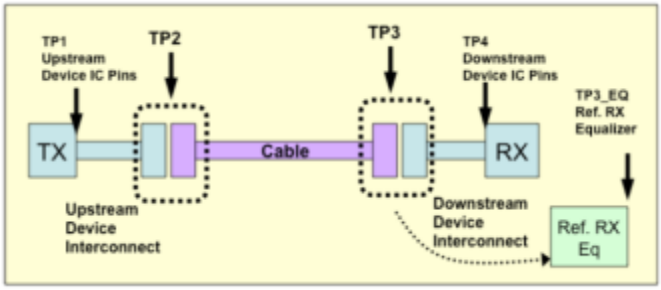
Ex) HPD Pulse

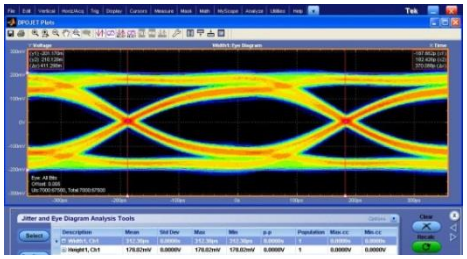


Define	Upon detection this "HPD IRQ Event"(0.5ms ~ 1ms) ,the source device must read the link / sink status field of the DPCD and take corrective action.

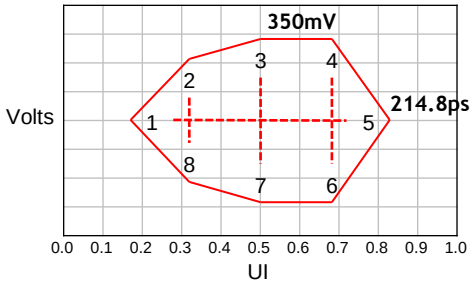
APPENDIX B. LGD Proposal for eDP Interface Design Guide

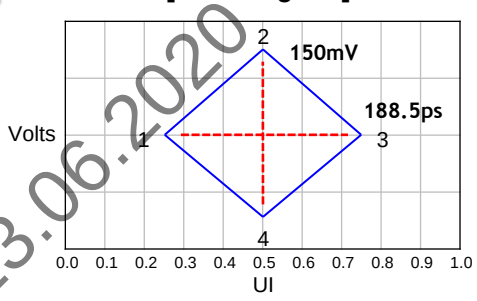
3 Main Link EYE Diagram





[EYE Diagram]





Point	UI	Voltage (Volts)
1	0.210	0.000
2	0.355	0.140
3	0.500	0.175
4	0.645	0.175
5	0.790	0.000
6	0.645	-0.175
7	0.500	-0.175
8	0.355	-0.140

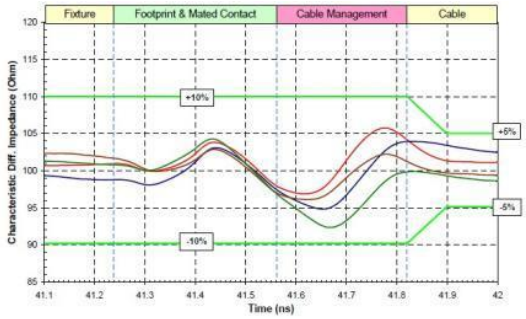
[EYE Vertices for TP2 at HBR]

Point	UI	Voltage (Volts)
1	0.246	0.000
2	0.500	0.075
3	0.755	0.000
4	0.500	-0.075

[EYE Vertices for TP3 at HBR]

Define	Main Link EYE Diagram should meet TP2 and TP3 point

4 Cable Impedance management

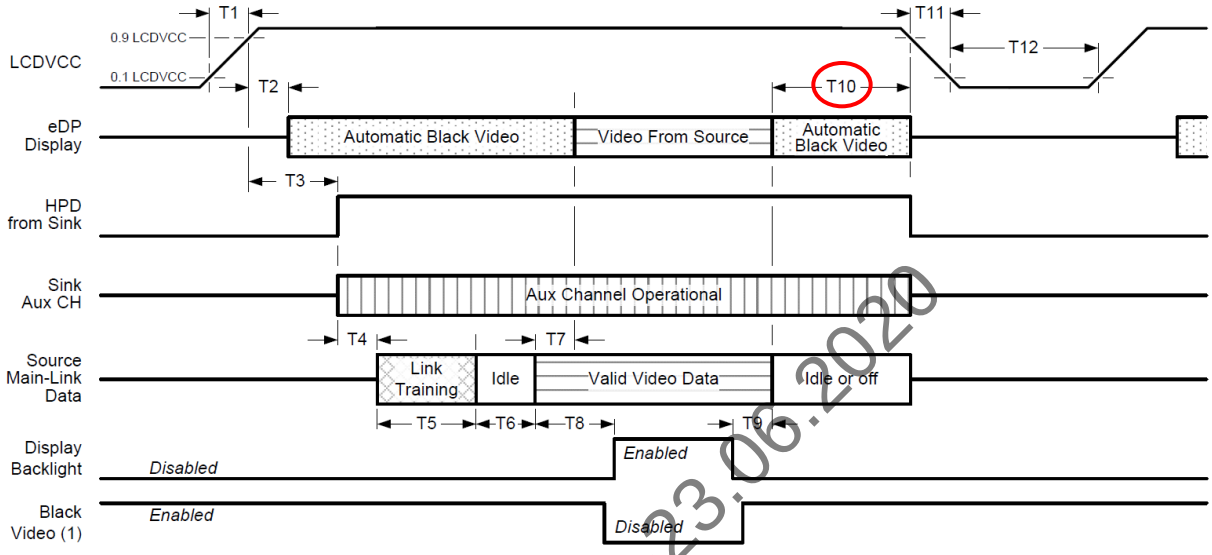


Segment	Differential Impedance	Maximum Tolerance
Fixture	100 Ω	+/- 10%
Connector	100 Ω	
Wire management	100 Ω	
Cable	100 Ω	+/- 5%

Define	Cable Impedance 100 Ω +/- 5% (95Ω ~ 105Ω)

APPENDIX B. LGD Proposal for eDP Interface Design Guide

5	Main Link Off vs. LCD Power Off at Non-PSR



Timing Parameter	Description	Required By	Min	Max
T10	Delay from end of valid video from Source to Power Off	Source	0ms	500ms

* LGD recommend that Source must power off the LCDVCC if Main Link off like below.

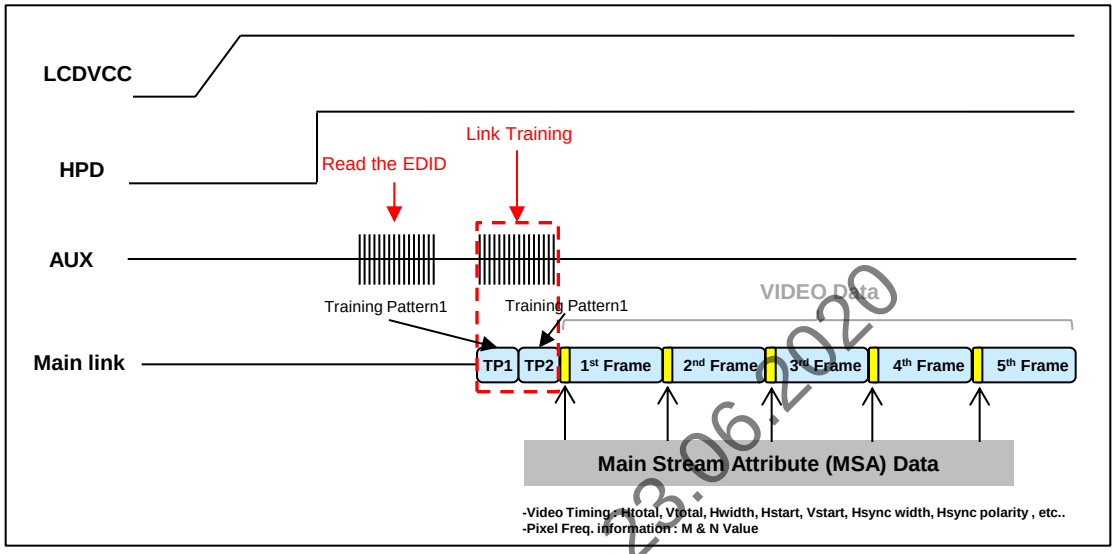
[Case1. Resolution Change]

[Case2. Close the Lid]

Define	If Main Link off signal from Source, then LCDVCC must be Power Off within T10 period at Non-PSR mode

APPENDIX B. LGD Proposal for eDP Interface Design Guide

6	Main Link M & N value of MSA data

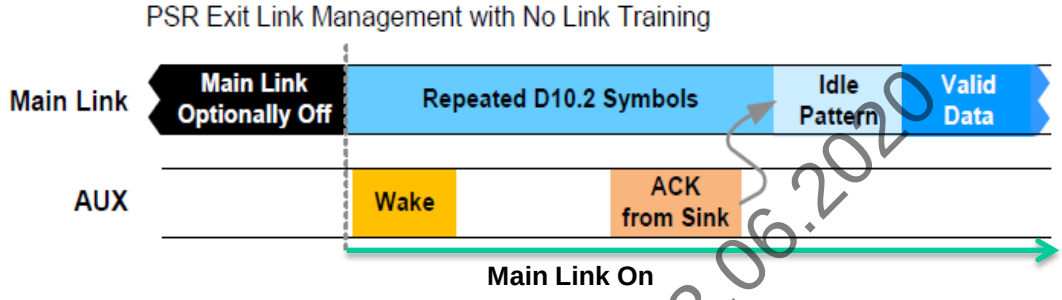


Define	It need to fix M& N value of MSA data output to prevent the initial abnormal M& N Value from incoming after power on.

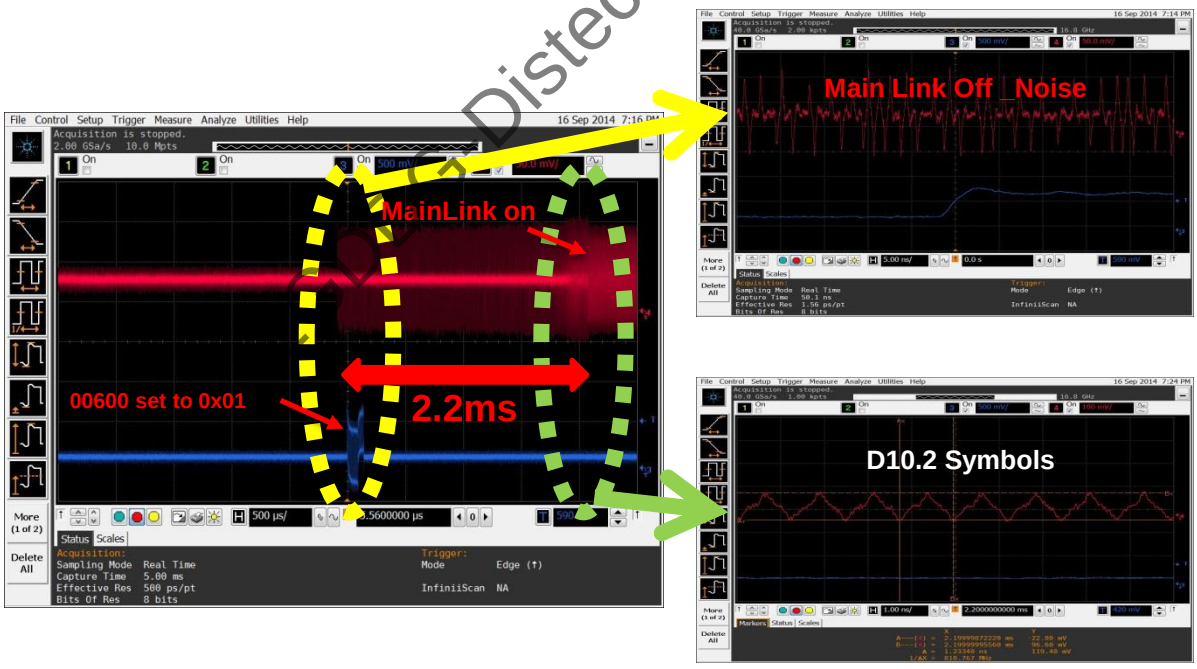
APPENDIX B. LGD Proposal for eDP Interface Design Guide

7	PSR Exit

If link training is not required, the Source must begin transmitting data on the Main Link prior to the wake AUX command which occurs through writing 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h; see *DP v1.2a*), as illustrated in the upper portion of Figure 6-9. This transmitted data must be a repetition of D10.2 symbols (which is the same as Link Training Pattern 1). Note the requirement above to transmit five repeats of the Idle Pattern after receiving ACK from the Sink.



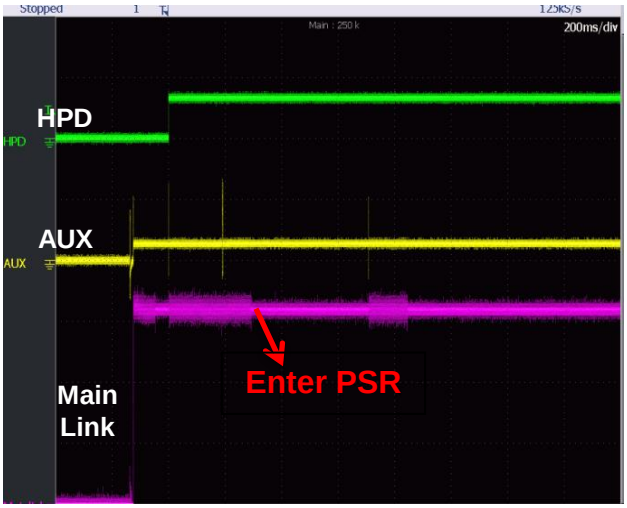
-. The below waveform is the issued case.



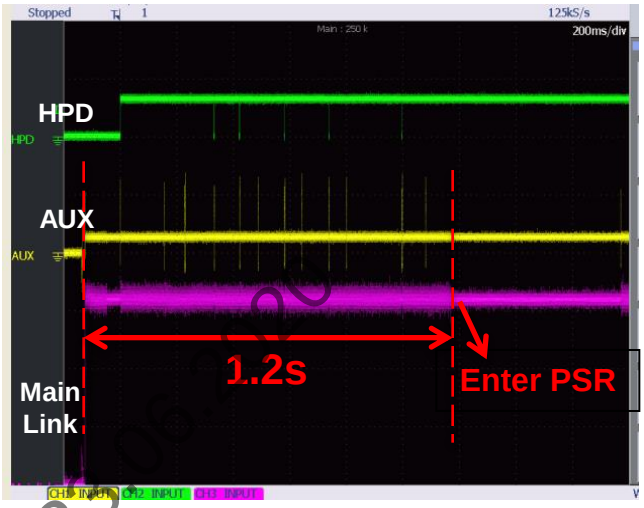
Define	If link training is not required, the source must begin transmitting data on the ML prior to the wake AUX wake-up command.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

8	1st time PSR Entry after Power on



< Issue waveform >



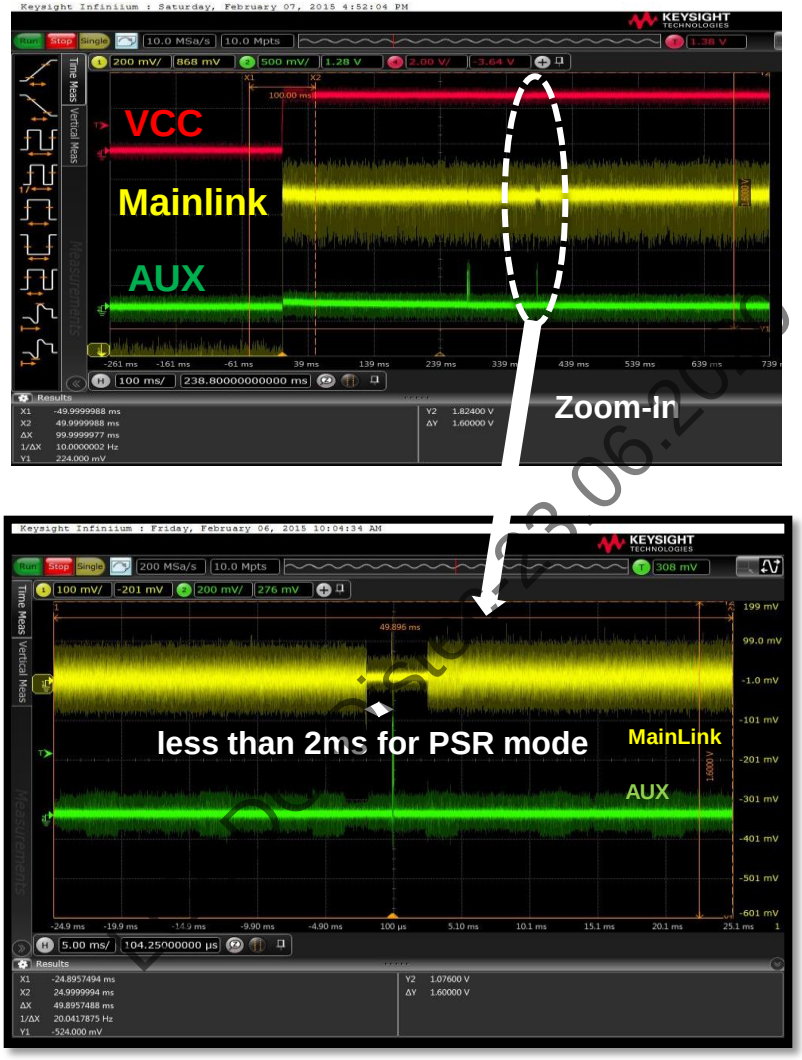
< solution waveform >

1. It is found that with solution , the TCON enter the PSR timing is 1.2s delay from VCC on which avoid TCON capture the wrong data from DP link(poor link quality) and enter the BIST mode + PSR mode(black screen).
2. **According to test, link is stable 800ms after VCC on.**

Define	After power(Vcc) on, the DP link is not stable, so the source try to PSR entry at 800ms after Power(Vcc) on.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

9	PSR Period Issue

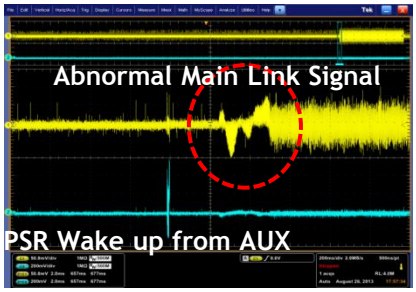


1. When issue is happened, system go to PSR mode for very short time.
2. If PSR active period is shorter than 1frame(16.67ms), T-Con can not go to the standby mode for PSR exit.

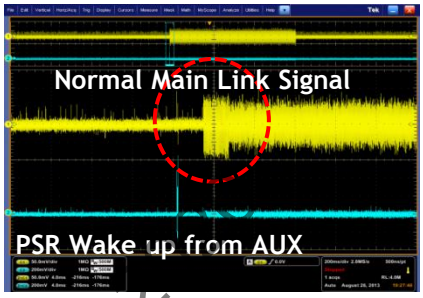
Define	When GPU go to the PSR mode, the source must hold the main link off over than 1frame.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

10	Main Link Noise at PSR Exit



[Abnormal Main Link Noise]



[Normal Main Link Signal]

Define	Main Link Noise at PSR Exit mode can be a cause abnormal display.

APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 1/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Header	0	**00**	Header	**00**	00000000
	1	**01**	Header	**FF**	11111111
	2	**02**	Header	**FF**	11111111
	3	**03**	Header	**FF**	11111111
	4	**04**	Header	**FF**	11111111
	5	**05**	Header	**FF**	11111111
	6	**06**	Header	**FF**	11111111
	7	**07**	Header	**00**	00000000
Vendor / Product EDID Version	8	**08**	ID Manufacture Name LGD	**30**	00110000
	9	**09**	ID Manufacture Name	**E4**	11100100
	10	**0A**	ID Product Code 0655h	**55**	01010101
	11	**0B**	(Hex. LSB first)	**06**	00000110
	12	**0C**	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	**00**	00000000
	13	**0D**	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	**00**	00000000
	14	**0E**	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	**00**	00000000
	15	**0F**	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	**00**	00000000
	16	**10**	Week of Manufacture - Optinal 00 weeks	**00**	00000000
	17	**11**	Year of Manufacture 2019 years	**1D**	00011101
	18	**12**	EDID structure version # = 1	**01**	00000001
	19	**13**	EDID revision # = 4	**04**	00000100
Display Parameters	20	**14**	Video input Definition = Input is a Digital Video signal Interface , Colo Bit Depth : 6 Bits per Primary Color , Digital Video Interface Standard Supported: DisplayPort is supported	**95**	10010101
	21	**15**	Horizontal Screen Size (Rounded cm) = 34 cm	**22**	00100010
	22	**16**	Vertical Screen Size (Rounded cm) = 19 cm	**13**	00010011
	23	**17**	Display Transfer Characteristic (Gamma) = (gamma*100)-100 = Example:(2.2*100)-100=120	**78**	01111000
	24	**18**	Feature Support [Display Power Management(DPM) : Standby Mode is supported, Suspend Mode is not supported, Active Off = Very Low Power is supported ,Supported Color Encoding Formats : RGB 4:4:4 & YCrCb 4:4:4 ,Other Feature Support Flags : No_sRGB, Preferred Timing Mode, No_Display is continuous frequency (Multi-mode_Base EDID and Extension Block).]	**EA**	11101010
Panel Color Coordinates	25	**19**	Red/Green Low Bits (RxRy/GxGy)	**38**	00111000
	26	**1A**	Blue/White Low Bits (BxBy/WxWy)	**D5**	11010101
	27	**1B**	Red X Rx = 0.590	**97**	10010111
	28	**1C**	Red Y Ry = 0.370	**5E**	01011110
	29	**1D**	Green X Gx = 0.350	**59**	01011001
	30	**1E**	Green Y Gy = 0.555	**8E**	10001110
	31	**1F**	Blue X Bx = 0.155	**27**	00100111
	32	**20**	Blue Y By = 0.110	**1C**	00011100
	33	**21**	White X Wx = 0.313	**50**	01010000
	34	**22**	White Y Wy = 0.329	**54**	01010100
Established Timings	35	**23**	Established timing 1 (Optional_00h if not used)	**00**	00000000
	36	**24**	Established timing 2 (Optional_00h if not used)	**00**	00000000
	37	**25**	Manufacturer's timings (Optional_00h if not used)	**00**	00000000
Standard Timing ID	38	**26**	Standard timing ID1 (Optional_01h if not used)	**01**	00000001
	39	**27**	Standard timing ID1 (Optional_01h if not used)	**01**	00000001
	40	**28**	Standard timing ID2 (Optional_01h if not used)	**01**	00000001
	41	**29**	Standard timing ID2 (Optional_01h if not used)	**01**	00000001
	42	**2A**	Standard timing ID3 (Optional_01h if not used)	**01**	00000001
	43	**2B**	Standard timing ID3 (Optional_01h if not used)	**01**	00000001
	44	**2C**	Standard timing ID4 (Optional_01h if not used)	**01**	00000001
	45	**2D**	Standard timing ID4 (Optional_01h if not used)	**01**	00000001
	46	**2E**	Standard timing ID5 (Optional_01h if not used)	**01**	00000001
	47	**2F**	Standard timing ID5 (Optional_01h if not used)	**01**	00000001
	48	**30**	Standard timing ID6 (Optional_01h if not used)	**01**	00000001
	49	**31**	Standard timing ID6 (Optional_01h if not used)	**01**	00000001
	50	**32**	Standard timing ID7 (Optional_01h if not used)	**01**	00000001
	51	**33**	Standard timing ID7 (Optional_01h if not used)	**01**	00000001
	52	**34**	Standard timing ID8 (Optional_01h if not used)	**01**	00000001
	53	**35**	Standard timing ID8 (Optional_01h if not used)	**01**	00000001

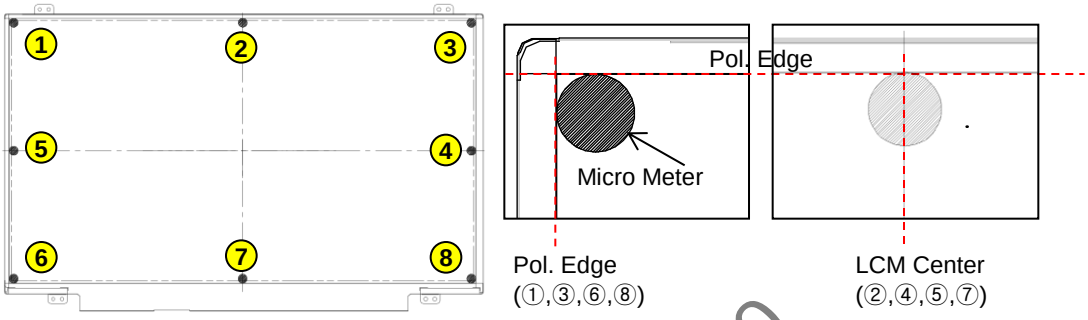
APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 2/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments		Value (Hex)	Value (Bin)
Timing Descriptor #1	54	**36**	Pixel Clock/10,000 (LSB)	138.7 MHz @ 60 Hz	**29**	00101001
	55	**37**	Pixel Clock/10,000 (MSB)		**36**	00110110
	56	**38**	Horizontal Active (HA) (lower 8 bits)	1920 pixels	**80**	10000000
	57	**39**	Horizontal Blanking (HB) (lower 8 bits)	160 pixels	**A0**	10100000
	58	**3A**	Horizontal Active (HA) / Horizontal Blanking (HB) (upper 4:4bits)		**70**	01110000
	59	**3B**	Vertical Avtive (VA)	1080 lines	**38**	00111000
	60	**3C**	Vertical Blanking (VB) (DE Blanking typ.for DE only panels)	31 lines	**1F**	00011111
	61	**3D**	Vertical Active (VA) / Vertical Blanking (VB) (upper 4:4bits)		**40**	01000000
	62	**3E**	Horizontal Front Porch in pixels (HF) (lower 8 bits)	48 pixels	**30**	00110000
	63	**3F**	Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits)	32 pixels	**20**	00100000
	64	**40**	Vertical Front Porch in lines (VF) : Vertical Sync Pluse Width in lines (VS) (lower 4 bits)	3 lines : 5 lines	**35**	00110101
	65	**41**	Horizontal Front Porch/ Sync Pulse Width/ Vertical Front Porch/ Sync Pulse Width (upper 2bits)		**00**	00000000
	66	**42**	Horizontal Vedio Image Size (mm) (lower 8 bits)	344 mm	**58**	01011000
	67	**43**	Vertical Vedio Image Size (mm) (lower 8 bits)	194 mm	**C2**	11000010
	68	**44**	Horizontal Image Size / Vertical Image Size (upper 4 bits)		**10**	00010000
	69	**45**	Horizontal Border = 0 (Zero for Notebook LCD)		**00**	00000000
	70	**46**	Vertical Border = 0 (Zero for Notebook LCD)		**00**	00000000
	71	**47**	Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_POS (outside of V-sync)]		**1A**	00011010
Timing Descriptor #2	72	**48**	Flag		**00**	00000000
	73	**49**	Flag		**00**	00000000
	74	**4A**	Flag		**00**	00000000
	75	**4B**	Data Type Tag (Descriptor Defined by manufacturer)		**00**	00000000
	76	**4C**	Flag		**00**	00000000
	77	**4D**	Descriptor Defined by manufacturer		**00**	00000000
	78	**4E**	Descriptor Defined by manufacturer		**00**	00000000
	79	**4F**	Descriptor Defined by manufacturer		**00**	00000000
	80	**50**	Descriptor Defined by manufacturer		**00**	00000000
	81	**51**	Descriptor Defined by manufacturer		**00**	00000000
	82	**52**	Descriptor Defined by manufacturer		**00**	00000000
	83	**53**	Descriptor Defined by manufacturer		**00**	00000000
	84	**54**	Descriptor Defined by manufacturer		**00**	00000000
	85	**55**	Descriptor Defined by manufacturer		**00**	00000000
	86	**56**	Descriptor Defined by manufacturer		**00**	00000000
	87	**57**	Descriptor Defined by manufacturer		**00**	00000000
	88	**58**	Descriptor Defined by manufacturer		**00**	00000000
	89	**59**	Descriptor Defined by manufacturer		**00**	00000000
Timing Descriptor #3	90	**5A**	Flag		**00**	00000000
	91	**5B**	Flag		**00**	00000000
	92	**5C**	Flag		**00**	00000000
	93	**5D**	Data Type Tag (Alphanumeric Data String (ASCII String))		**FE**	11111110
	94	**5E**	Flag		**00**	00000000
	95	**5F**	Alphanumeric Data String (ASCII String)	L	**4C**	01001100
	96	**60**	Alphanumeric Data String (ASCII String)	G	**47**	01000111
	97	**61**	Alphanumeric Data String (ASCII String)		**20**	00100000
	98	**62**	Alphanumeric Data String (ASCII String)	D	**44**	01000100
	99	**63**	Alphanumeric Data String (ASCII String)	i	**69**	01101001
	100	**64**	Alphanumeric Data String (ASCII String)	s	**73**	01110011
	101	**65**	Alphanumeric Data String (ASCII String)	p	**70**	01110000
	102	**66**	Alphanumeric Data String (ASCII String)	l	**6C**	01101100
	103	**67**	Alphanumeric Data String (ASCII String)	a	**61**	01100001
	104	**68**	Alphanumeric Data String (ASCII String)	y	**79**	01111001
	105	**69**	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASCⅡ code 0Ah,set remaining char = 20h)		**0A**	00001010
	106	**6A**	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASCⅡ code 0Ah,set remaining char = 20h)		**20**	00100000
	107	**6B**	Manufacturer P/N(If<13 char--> 0Ah, then terminate with ASCⅡ code 0Ah,set remaining char = 20h)		**20**	00100000

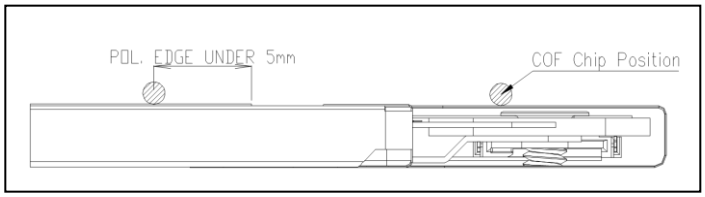
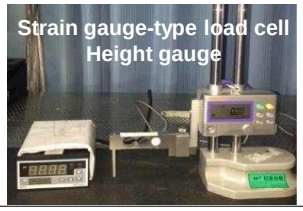
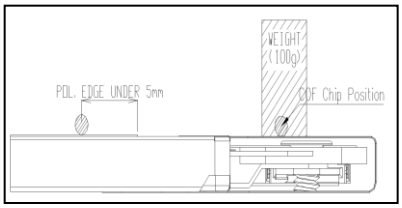
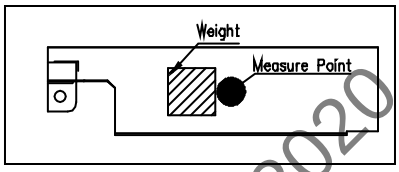
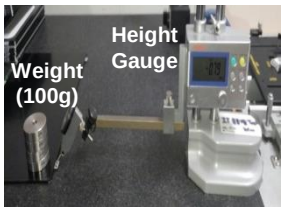
APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 3/3

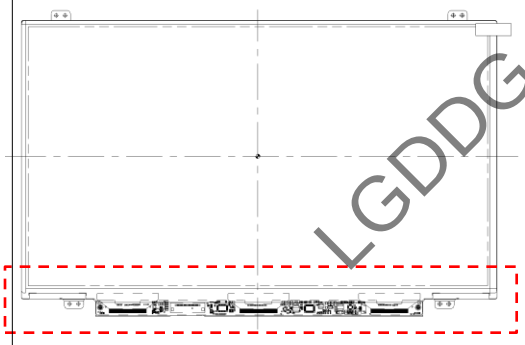
	Byte (Dec)	Byte (Hex)	Field Name and Comments		Value (Hex)	Value (Bin)
Timing Descriptor #4	108	**6C**	Flag		**00**	00000000
	109	**6D**	Flag		**00**	00000000
	110	**6E**	Flag		**00**	00000000
	111	**6F**	Data Type Tag (Alphanumeric Data String (ASCII String))		**FE**	11111110
	112	**70**	Flag		**00**	00000000
	113	**71**	Alphanumeric Data String (ASCII String)	L	**4C**	01001100
	114	**72**	Alphanumeric Data String (ASCII String)	P	**50**	01010000
	115	**73**	Alphanumeric Data String (ASCII String)	1	**31**	00110001
	116	**74**	Alphanumeric Data String (ASCII String)	5	**35**	00110101
	117	**75**	Alphanumeric Data String (ASCII String)	6	**36**	00110110
	118	**76**	Alphanumeric Data String (ASCII String)	W	**57**	01010111
	119	**77**	Alphanumeric Data String (ASCII String)	F	**46**	01000110
	120	**78**	Alphanumeric Data String (ASCII String)	D	**44**	01000100
	121	**79**	Alphanumeric Data String (ASCII String)	-	**2D**	00101101
	122	**7A**	Alphanumeric Data String (ASCII String)	S	**53**	01010011
	123	**7B**	Alphanumeric Data String (ASCII String)	P	**50**	01010000
	124	**7C**	Alphanumeric Data String (ASCII String)	M	**4D**	01001101
	125	**7D**	Alphanumeric Data String (ASCII String)	2	**32**	00110010
Checksum	126	**7E**	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)		**00**	00000000
	127	**7F**	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)		**E3**	11100011

APPENDIX D. LGD Proposal for Measurement Method

1	LCM Thickness
Point	
Measure Tool	Micro Meter  
Guide	✓ Measure the thickness between Polarizer surface and M-Chassis on the rear of LCM ✓ Subtract Pol. protect film thickness from LCM thickness

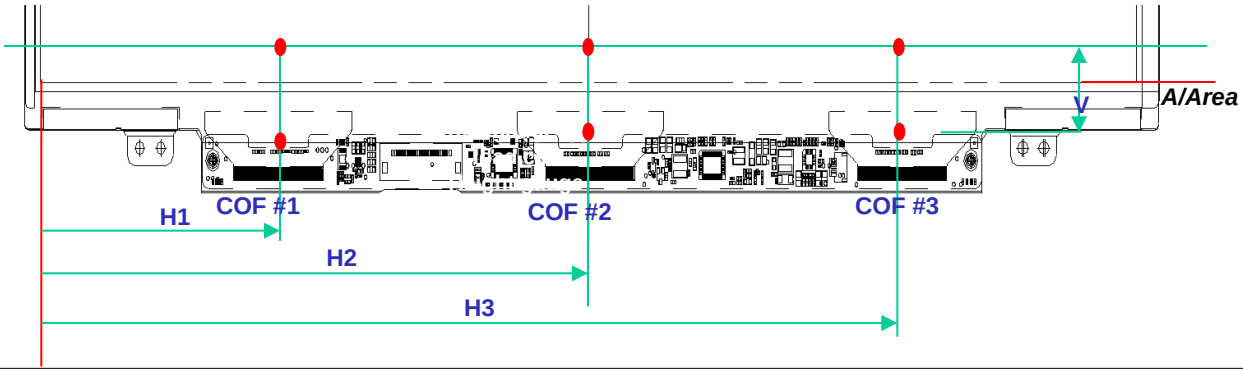
APPENDIX D. LGD Proposal for Measurement Method

4	Height of PCB Area
Measure Tool & Point	 
Measure Tool & Point	  
Guide	✓ Measure the height between upper Polarizer surface and C/Shield top surface. ✓ Measure the height include force(100gf) on the C/Shield surface at FPC/COF Center. ✓ The CAS Spec. : All components except cover shield of LCM is under upper POL. Upper polarizer higher than source cover shield pressed down 100g.
Measure condition	Put the LCM on flat ground w/o interference on PCB rear side



※ Measure Point

Item	Description
Measure Tool	Height gauge (with Strain gauge type load-cell or weight)
Measure Point	V-dimension : Pol. Edge ~ 5mm, FPC/COF Center(or Chip) H-dimension : Each FPC/COF Center(or Chip) → Including all of components on PCB



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